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AN5639

Application note

Flicker extraction using VD6283

Introduction

This document describes how artificial light flicker is extracted using VD6283.

1 Acronyms and abbreviations

Acronym/abbreviation	Definition
ADC	analog-to-digital converter
DC	direct current
FFT	Fast Fourier transform
I2C	inter-integrated circuit
IES	Illuminating Engineering Society
LED	light emitting diodes
PDM	pulse density modulation
Rp	resistance pull-up
Rs	series resistor

2 What is flicker

2.1 Flicker definition

Optical flicker is defined as the pulsating or fluctuating light phenomenon of artificial light sources.

At low frequency flicker is visible (the human eye can detect the blinking of the light). Above 100 Hz optical flicker is no longer visible by the human eye, but it is still present and still may have effects on humans.

Most types of artificial lights emit flicker when connected to the power mains (home or business office) which is mainly 50 Hz or 60 Hz depending on the country.

Due to the current alternating its flow through the light, all artificial lights emit a flicker frequency at 100 Hz or 120 Hz, respectively for 50 Hz and 60 Hz power mains.

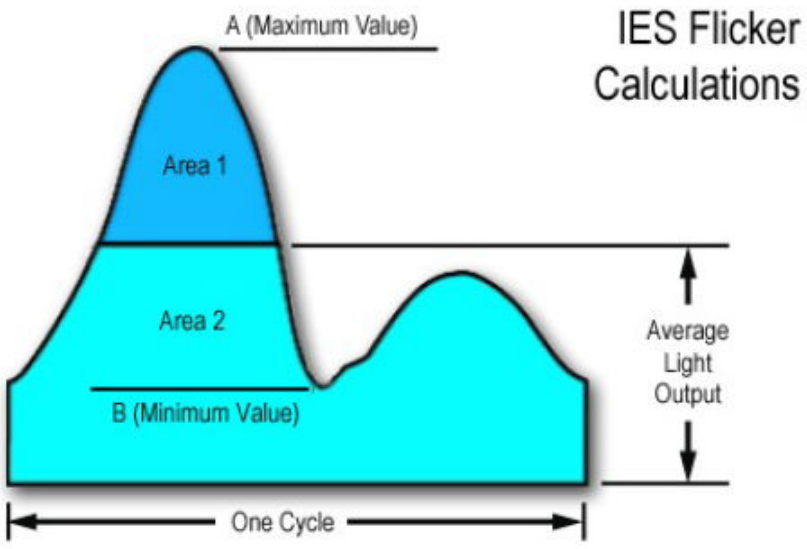
In order to remove a visible flicker and reduce the effects on humans, most light emitting diodes (LED) use a PWM dimming method in order to have a higher flicker frequency.

The VD6283 sensor can detect light flicker frequencies up to 2 kHz.

2.2 Flicker metrics

The following illustration is extracted from IES.org.

Figure 1. IES flicker calculations



2.2.1 Percent flicker

The percent flicker is an IES definition. It is a well known metric based on a scale from 0% to 100%.

This scale varies with light peak-to-peak amplitude and average. It is sometimes referred to as modulation depth.

$$Percent\ flicker\ = 100\,\%\ \times \frac{A-B}{A+B}$$

A visual way to represent the percent flicker is the amplitude level around a DC level (current (A) or voltage (V)), and using the following formulas:

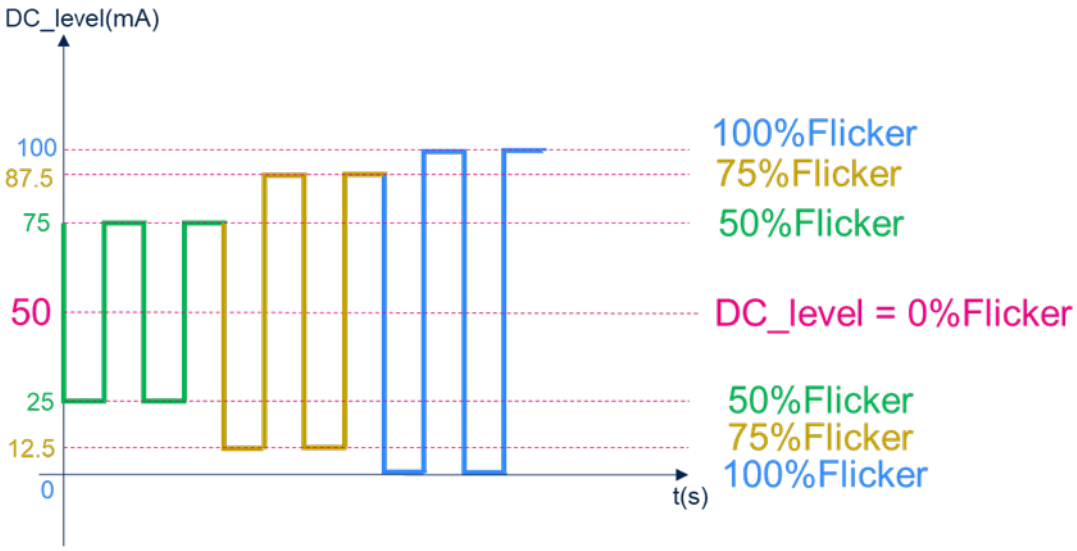
$A_0 = DC_{level}$ - %Flicker x DC_{level}

$A_1 = DC_{level}$ + %Flicker x DC_{level}

Figure 2. **Flicker amplitude**

Example: Taking a DC _level at 50 mA, various percent flicker is represented as followed:

Figure 3. **Percent flicker example at DC = 50 mA**



Note: Signal waveform and Duty cycle are not considered in the percent flicker metric (1 dimensional only).

2.2.2 Flicker index

The flicker index is a new metric based on a scale from 0 to 1.0. Flicker index, as defined by IES.org, "is a measure of the cyclic variation in output of a light source, taking into account the waveform of the light output. It is the ratio of the area under the light output curve that is above the average light output level to the total area under the light output curve for a single cycle."

This flicker index is independent of the frequency, the light variation, the amplitude, the shape (square or sinus), and the duty cycle.

$$Flicker\ Index = \frac{Area1}{Area1 + Area2}$$

2.3 VD6283 flicker operating characteristics

Table 1. Flicker operating characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Percent flicker ranges	White LED, 4000 K (DC level) from 1 to 5 Lux	20	—	100	%
	White LED, 4000 K (DC level) from 5 to 4000 Lux	3	—	100	
AC flicker frequency detection range	For above percent flicker ranges	100	—	2000	Hz
AC flicker frequency detection accuracy	Frequency range = 100 Hz to 2000 Hz Light waveform = square (PWM)	3	1	3.3	%
	Frequency range 100= 100 Hz / 120 Hz Light waveform = sine wave		1	3.3	

3 Flicker extraction - Hardware configuration

Flicker frequency can be extracted out of the VD6283 modules in analog or digital mode.

The I²C bus can be configure in fast mode or fast mode plus:

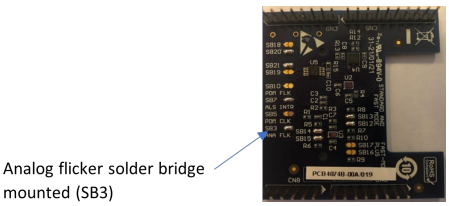
- For I²C 400 kHz (fast mode), the recommended master pull-up (Rp) is 2.2 kohm, and serial resistors = 0 ohm. All must be placed close to the host.
- For I²C 1 MHz (fast mode plus), series resistor (Rs) usage is recommended as per the I²C bus specification. Please refer to the datasheet.
- All capacitors should be placed as close as possible to VDD and VSS pins.

The flicker can be extracted by FFT. This method allows 100 Hz to 2 kHz flicker detection, and detection of multi-tone frequencies.

By default, the expansion board is configured in flicker analog mode. The solder bridge 3 (SB3) is mounted.

3.1 Analog mode

Figure 4. Analog flicker solder bridge mounted



The PDM signal is routed out of GPIO2 and filtered by an external RC filter to get a continuous analog signal.

To do the extraction in analog mode, connect the VD6283 flicker signal to an ADC module (that is, host or other).

An external RC filtering is required before connecting the ADC input.

Figure 5. Analog mode schematic

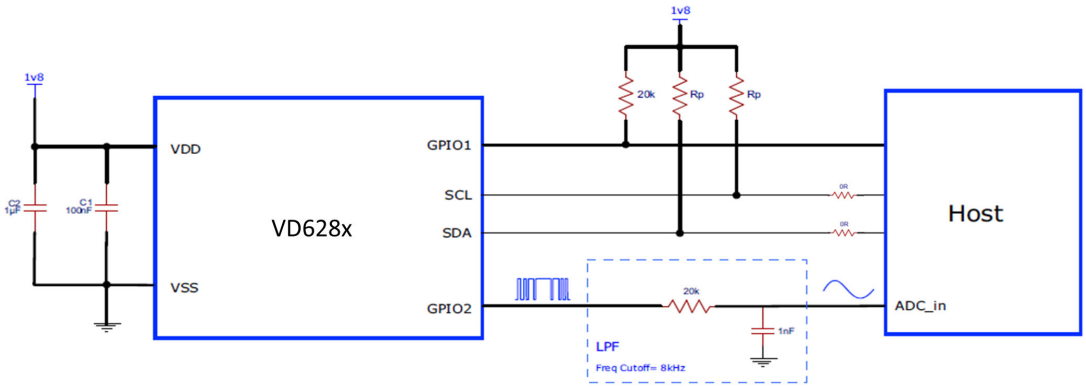
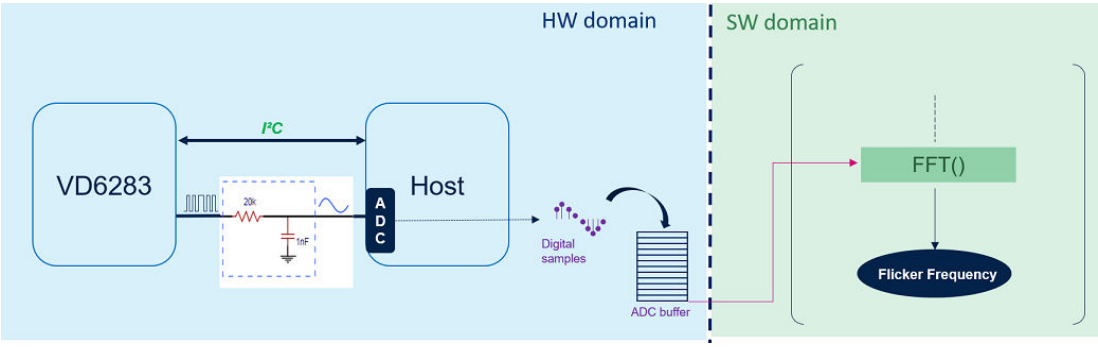


Figure 6. **VD6283 flicker extraction with ADC**



3.2 Digital mode

To configure the flicker in digital mode, unsolder the SB3 and mount the solder bridge SB10.
Raw data is output in digital format through the GPIO1 pin.
The host must input a master clock (2 MHz to 10 MHz) into GPIO2 to synchronize the data stream.
Either host SPI or PDM port can be used in this mode.

Figure 7. **Digital flicker solder bridge mounted**

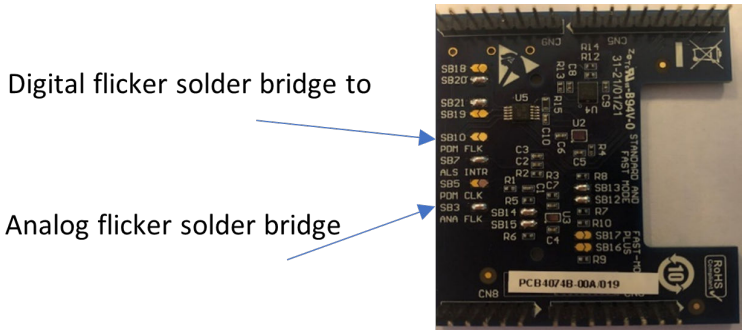


Figure 8. **Digital mode schematic**

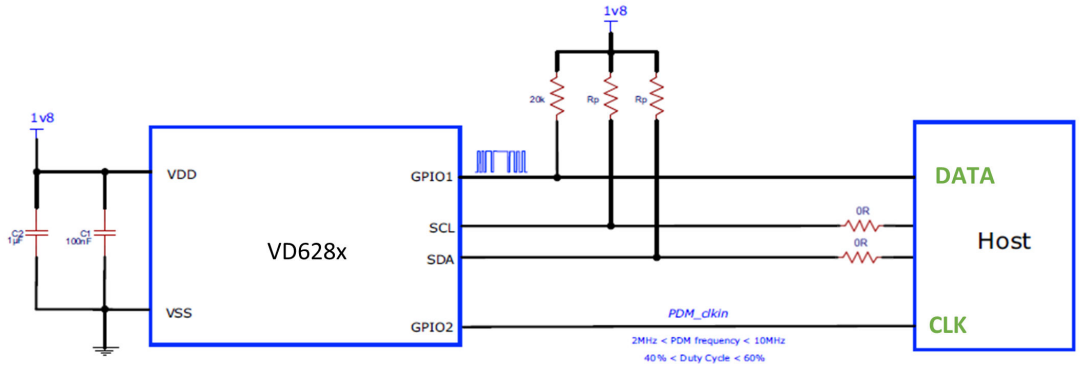
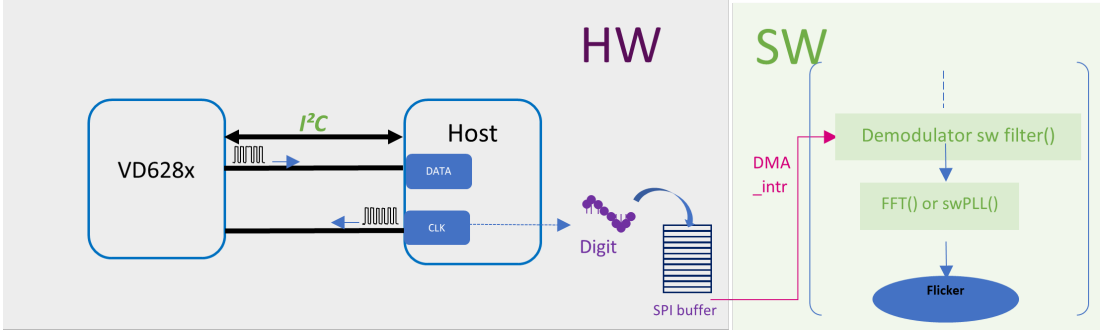


Figure 9. **VD6283 flicker extraction with SPI**



4 Application in the VD6283 module

4.1 Pedestal value

For some lights with very low DC level and low duty cycle, it can be difficult to extract flicker frequency.

To improve the accuracy, a pedestal option can be activated. It creates a periodic “spurious” pulse, to force conversion and have data output through the PDM signal.

The pedestal activation and control can be done in the following register:

Table 2. Pedestal registers

Name	Reg address	Function	Reg value
AC_MODE	31	Pedestal on/off	0: pedestal added to help flicker in very low DC conditions 1: remove pedestal feature
AC_PEDESTAL	32	pedestal_value	Pedestal_value (default = 5) 0: 2^0 x 256 clock cycles (10.24MHz) between pulses 1: 2^1 x 256 clock cycles (10.24MHz) between pulses ... 7: 2^7 x 256 clock cycles (10.24MHz) between pulses

Note: The recommended value to be used for AC_PEDESTAL is 3.

4.2 Pseudo code flicker analog

```
CustomerPrivate client;
void *hdl;

// sensor initialization
Error = STALS_Init("VD6283", &client, &hdl);

// First configure sensor settings
Error = STALS_SetGain(hdl, STALS_CHANNEL_6, 0x0a00, &current_gain);
Error = STALS_SetFlickerOutputType(hdl, STALS_FLICKER_OUTPUT_ANALOG);

// start Flicker sampling
Error = STALS_Start(hdl, STALS_MODE_FLICKER, STALS_CHANNEL_6);

// capture data from GPIO2 pin through an external RC filter using a platform dependent adc
// Sampling frequency must be greater than 4Khz

Platform_capture_adc(data);
Platform_fft(data, data_fft);
flk_frequency = Platform_flk_detect(data_fft);
printf("flicker frequency %d hz\n", flk_frequency);

// stop acquisition
Error = STALS_Stop(hdl, STALS_MODE_FLICKER);

// Release sensor
Error = STALS_Term(&hdl);
```

4.3 Pseudo code flicker digital

```
CustomerPrivate client;
void *hdl;

// sensor initialization
Error = STALS_Init("VD6283", &client, &hdl);

// First configure sensor settings
Error = STALS_SetGain(hdl, STALS_CHANNEL_6, 0x0a00, &current_gain);
Error = STALS_SetFlickerOutputType(hdl, STALS_FLICKER_OUTPUT_DIGITAL_PDM);

// start Flicker sampling
Error = STALS_Start(hdl, STALS_MODE_FLICKER, STALS_CHANNEL_6);
platform_spi_start(client, &fe)

// capture data from GPIO1 pin through using a SPI bus or Audio codec.
// Sampling frequency must be greater than 4Khz

Platform_spi_get_frame(data);
Platform_fft(data, data_fft);
flk_frequency = Platform_flk_detect(data_fft);
printf("flicker frequency %d hz\n", flk_frequency);

// stop acquisition
platform_spi_stop(client);
Error = STALS_Stop(hdl, STALS_MODE_FLICKER);

// Release sensor
Error = STALS_Term(&hdl);
```

Revision history

Table 3. **Document revision history**

Date	Version	Changes
06-Jul-2021	1	Initial release
25-Mar-2024	2	Added digital mode to Section 3: Flicker extraction - Hardware configuration, including new subsection Section 3.2: Digital mode. Updated Section 4.1: Pedestal value, including adding more information for the AC_PEDESTAL reg value. Added Section 4.3: Pseudo code flicker digital.