Application note

GaN transistors gate driving solutions

Introduction

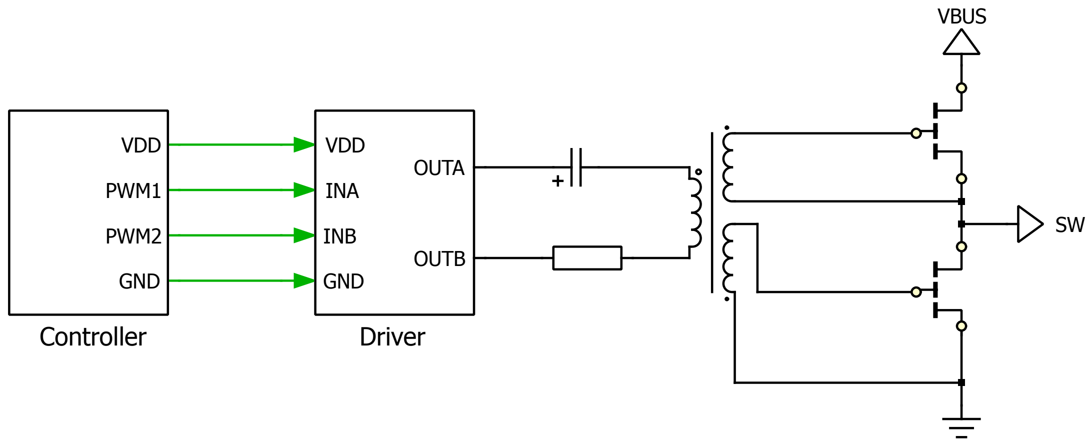
In switching-mode power supplies (SMPS), most topologies require at least a half-bridge to switch the voltage applied to an inductor or transformer. Ensuring isolation between the controller and the power switches is crucial for safe and reliable operation. We start by introducing the standard solution using pulse transformers, commonly used with traditional Si MOSFETs, and then explore various solutions based on gate drivers with different power supply implementations.

This application note aims to review key solutions for driving the gate of gallium nitride (GaN) devices to enhance robustness, power density, and overall efficiency. The comparison includes typical schematics along with PCB layout recommendations. Additionally, gate waveforms from a standard double pulse (DP) test are presented.

1 Pulse transformer (solution 1)

The pulse transformer is the most commonly used solution for driving a switch in a half-bridge leg. This well-known component is cost-effective and provides galvanic isolation. However, it requires a dual-channel driver to apply a positive voltage on the primary winding during the first half of the period and a negative voltage in the second half. Thanks to that, we insure that its core flux is well reset. By aware that some solutions with additional components around the pulse transformer exist to get a rid of this 50 % duty cycle limit.

Figure 1. Dual channel driver + pulse transformer



As mentioned in the introduction, this solution is typically used with MOSFETs. However, the fast dv/dt and di/dt characteristics of GaN technology expose the limitations of pulse transformers. The intrinsic pulse transformer leakage inductance combined with GaN fast switching can lead to oscillation on the gate and, at the end, potential shoot-through due to unexpected turn-on.

Moreover, the voltage-time area (E-T) imposes a minimum switching frequency. For example, when driving a GaN device with a ±6 V swing (12 V total), a transformer with an E-T value of 80 V/µs would result in a minimum switching frequency of 75 kHz. Applications with lower frequencies would require a larger transformer with a higher E-T parameter.

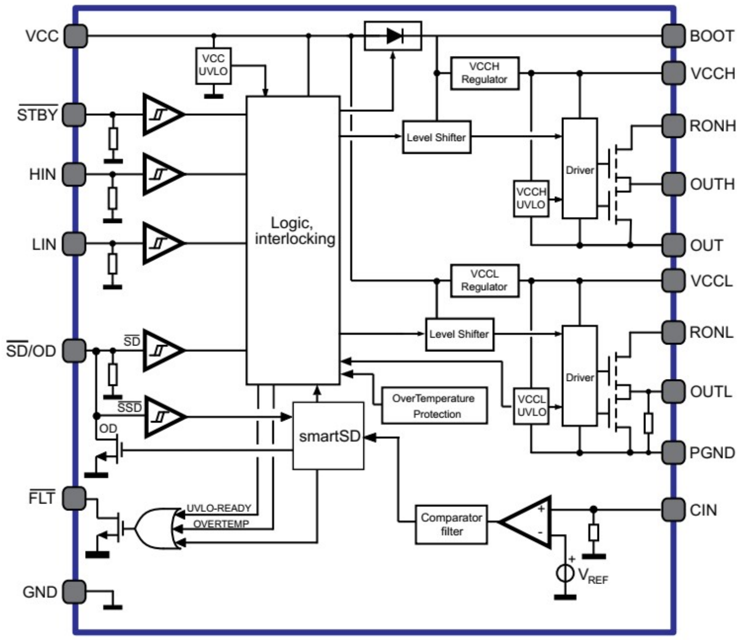
This configuration is not tested in this document due to the aforementioned limitations.

2 Driver with embedded bootstrap diode (solution 2)

The most challenging aspect of driving a half-bridge leg is managing the high-side switch. Since this component is floating and not referenced to the ground, a special implementation is necessary. The STDRIVEG611 is one such solution (see Figure 1).

This device can drive both low and high-side switches in a compact QFN4x5x1 package. It is tailored for GaN technology, offering a lower UVLO threshold (compared to SiC or Si MOSFETs), high immunity to transient dv/dt (±200 V/ns), and the ability to achieve high switching frequencies (> 1 MHz).

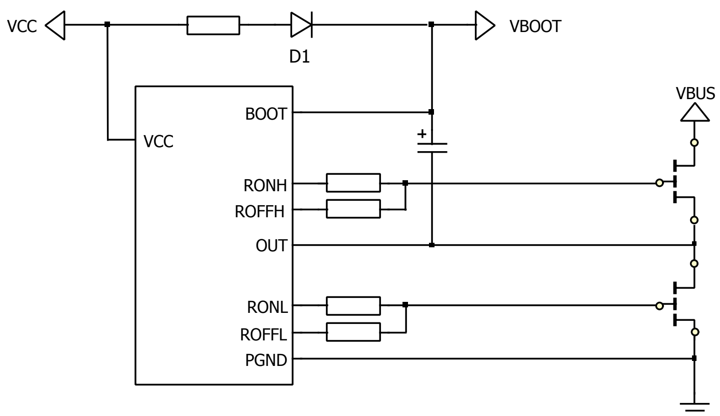
Figure 2. STDRIVEG611 block diagram



Let us discuss the power supply. As previously mentioned, driving the low-side switch is straightforward since its source terminal is referenced to the ground of the IC. However, the high-side switch is floating, and this driver includes an embedded bootstrap diode.

- **How does it work?**: You can refer to the Figure 3, which shows the typical bootstrap network schematic.

Figure 3. Simplified bootstrap schematic for high side power supply



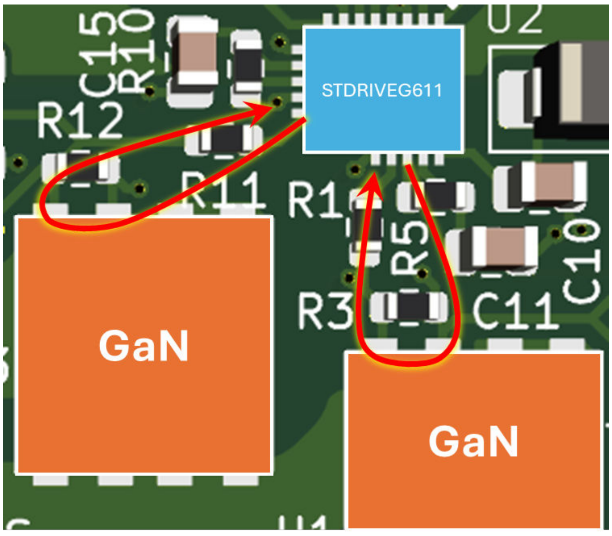
The bootstrap network primarily consists of a high voltage diode connected between the V_{CC} pin and the boot pin. Additionally, a capacitor is connected between the boot pin and the switching node, referred to as OUT for this IC. When the low-side switch is turned on, the OUT pin is brought to the same potential as the ground. During this phase, the bootstrap capacitor charges to the V_{CC} voltage level, minus the diode voltage drop.

Another key block of this driver is the V_{CC} regulator (Figure 2). This function ensures that the supply voltage for the high-side structure is well regulated to 6 V. Since the on-time duration varies depending on conditions such as line voltage and load, the time during which the capacitor needs to supply the high-side driver also varies. This is particularly relevant in PFC applications. Without a regulator, the voltage must be set below the maximum voltage accepted by the GaN device (7 V in our case). Considering some margin, 6 V is a good trade-off. In a TTPFC, the duty cycle can vary between 0 % and nearly 100 %, which could affect the bootstrap capacitor voltage. Having a regulator prevents supply voltage variations and ensures optimal GaN drive.

You can see the high side block is connected through a level shifter (with the noise immunity mentioned earlier) in order to sustain the high voltage offset.

Regarding the PCB layout, the small package size allows the driver to be placed as close as possible to the switches. The picture below shows a possible implementation with a PF8x8 bottom side cooling (BSC) package. The loop around the gate must be optimized to avoid ringing and unexpected shoot-through.

Figure 4. Gate drive layout example with STDRIVEG611

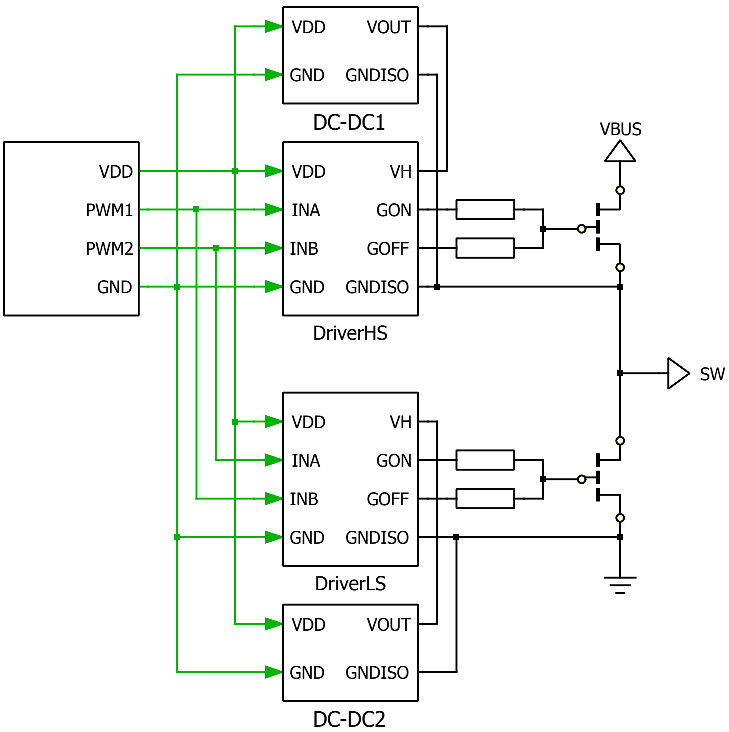


3 Single driver with embedded galvanic isolation and DC-DC power supply (solution 3)

To provide more flexibility for designers, two single drivers with embedded galvanic isolation can be used. During the design phase, physical constraints such as cooling systems (air or water cooling) or mechanical holes for attaching the PCB to the enclosure may arise. As a result, in a half-bridge configuration, both power switches might be positioned "far apart," even though the power loop should be minimized. Using single drivers allows the driving loop to be optimized with a short distance between the driver, gate resistance ($R_{G(ON)}$ and $R_{G(OFF)}$), and the gate pin itself. This approach offers significant flexibility for PCB layout, simplifying trace routing. It also facilitates parallelization, with one dedicated driver for all low- or high-side power switches.

In ST's product portfolio, the STGAP2GS is a single gate driver designed specifically for GaN technology. This component has separate sink and source pins to optimize turn-on and turn-off transitions, with high current capability for parallelization configurations (2 A source and 3 A sink).

Figure 5. Two single drivers with embedded galvanic isolation and isolated DC-DC



In the schematic shown in Figure 5, it is important to note that the secondary side of the driver requires an isolated power supply to maintain galvanic isolation. Several solutions can be used to generate the required voltage. One option is to use an isolated DC-DC module. Modules like the Murata NXJ family offer a variety of configurations for input and output voltages, ranging from 5 V to 12 V, with everything integrated.

To drive properly the GaN device, STMicroelectronics recommends supplying the gate with voltages between -3 V and +6 V. The on-state threshold ensures a full turn-on of the GaN device with sufficient margin below the maximum gate voltage limit of 7 V. The negative voltage is recommended to provide adequate margin between the off-state voltage and the V_{TH} threshold, which is lower for GaN compared to traditional Si MOSFETs. This negative voltage can be easily generated using simple Zener diodes, as illustrated in Figure 6.

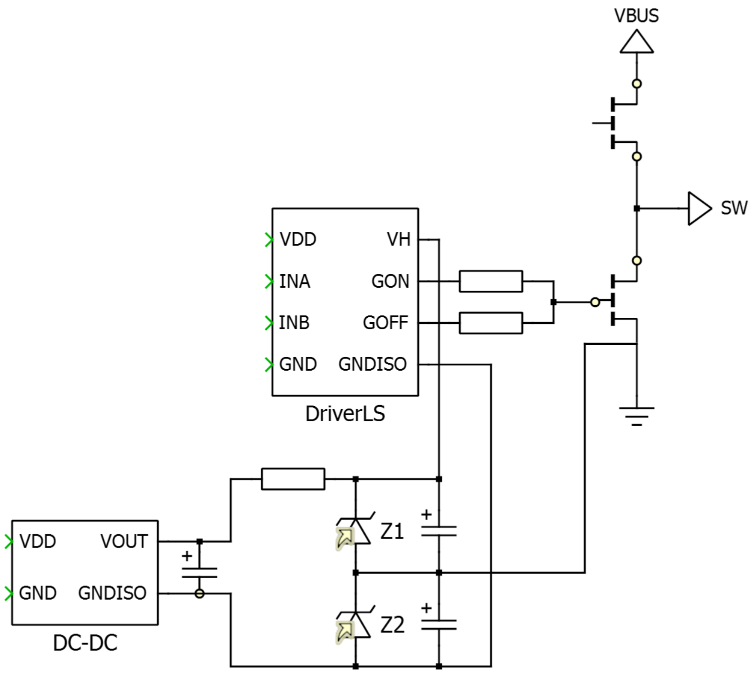


Figure 6. **Simple Zener diodes to generate a negative voltage**

The output voltage is split into two parts to create a positive 6.2 V (using a 6.2 V Zener diode, Z1) and a negative 3 V (using a 3 V Zener diode, Z2). The series resistor sets the correct bias current to ensure a stable voltage. Typically, a 390 Ω resistor is sufficient for ST GaN devices.

The isolated Dc-Dc module is a convenient, ready-made solution, though it comes at a certain cost. An isolated power supply can also be created using a pulse transformer.

- **How does it work**?: The schematic is shown in Figure 7

The transformer requires an AC signal on the primary winding. With the help of driver IC1, the 12-V DC voltage is converted to a -6 V/+6 V square wave signal, assisted by the PWM_aux signal (for example, 90 kHz, 50 % duty cycle) and capacitor C1, which removes the DC component. The transformer, with a 1:1 turns ratio, delivers a -6 V/+6 V square wave signal. Finally, diodes D1 and D2 isolate the negative and positive voltages to supply the secondary side of the isolated driver STGAP2GS.

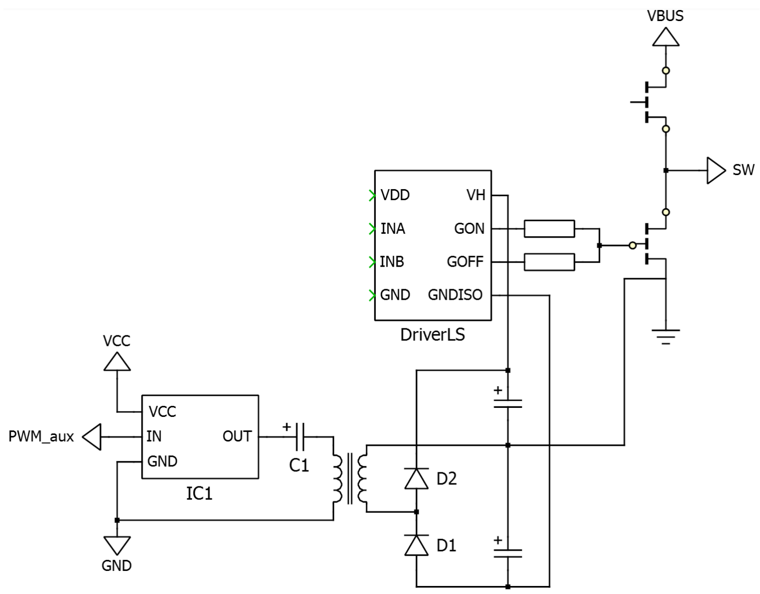
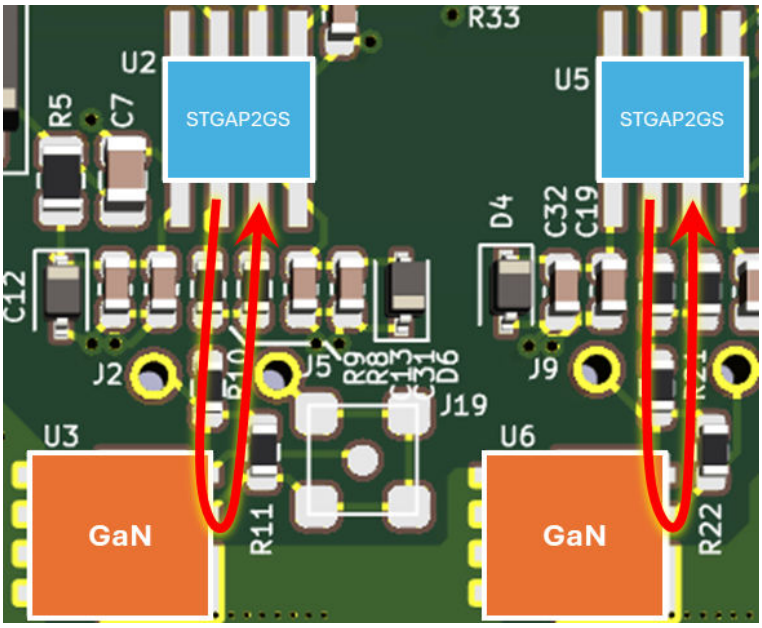


Figure 7. **Alternative to the isolated DC-DC power supply**

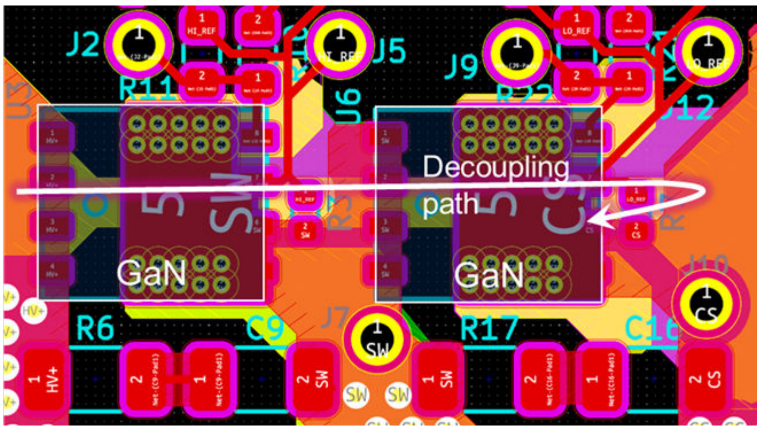
As mentioned earlier, having a dedicated driver for each GaN device provides substantial flexibility in PCB layout. Figure 8 illustrates another possible layout implementation using the STGAP2GS driver, which is specifically designed for GaN devices.

Figure 8. Gate loop layout example with STGAP2GS driver



Each driver is placed as close as possible to the gate pin to optimize the driving loop for both devices. With this arrangement and the use of bottom-side cooling (BSC) packages (PF8x8 or PF5x6), both devices can be positioned side by side. Since PowerGaN transistors are used for high power and copper zones are typically used to conduct the current, the flux cancellation principle must be applied to reduce parasitic inductance. When two planes are face-to-face and conduct equal but opposite currents, the fluxes created by the currents cancel each other, effectively eliminating inductance. As illustrated in Figure 9, using the first inner layer as a power loop return path, just below the top layer, allows for a small loop size and reduced parasitic inductance due to field self-cancellation.

Figure 9. Power loop layout example using GaN PF5x6 package



This layout example, with a BSC cooling package and a single isolated driver, provides the optimal combination for enhancing both the drive and power loops.

4 Comparison

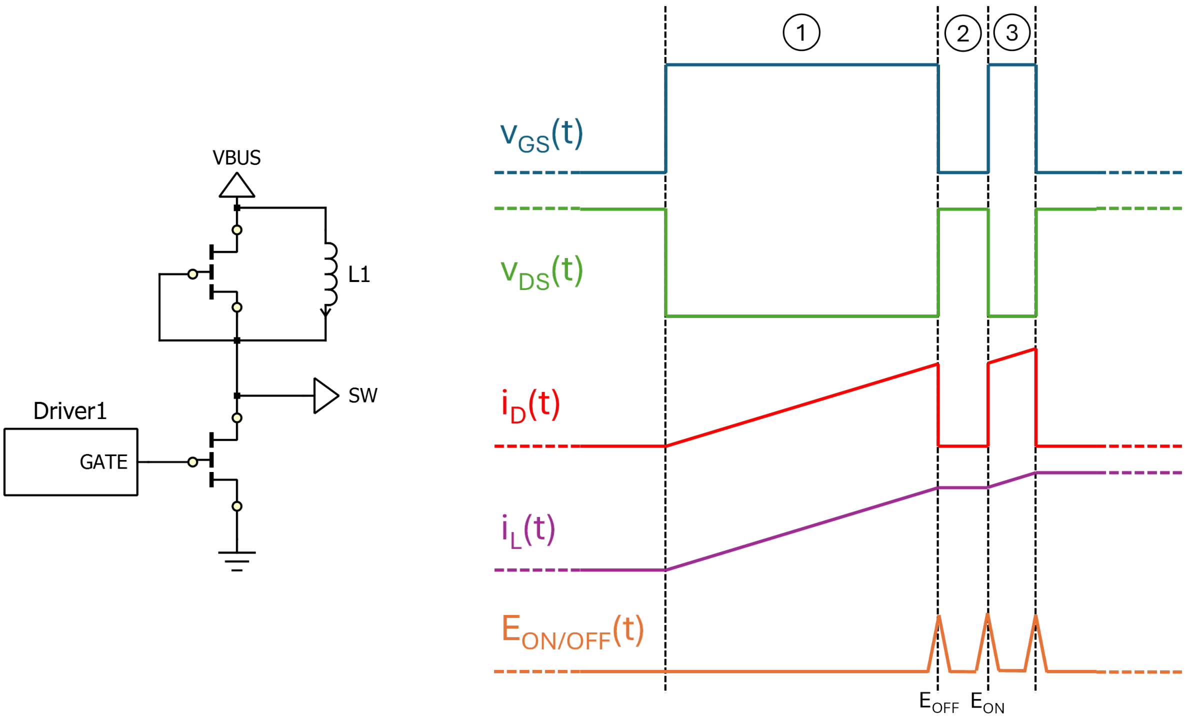
- What do the waveforms look like for the solutions presented above?
- Why not use the double pulse (DP) test method?

The double pulse test is a widely used technique for characterizing the switching behavior of power semiconductor devices such as MOSFETs, IGBTs, SiC, and GaN transistors. This test is essential for understanding the dynamic performance, switching losses, and efficiency of these devices in power electronic circuits.

The test procedure can be divided into three main phases (Figure 10):

1. Initially, the first pulse is generated by turning on the low-side device. Current begins to flow through the device and the load inductor, ramping up to a specified value where all parameters need to be extract
2. During the next step, the gate driver turns off the device for a short period. The current freewheels through the freewheeling diode (if present) or the high-side device (reverse conduction mode)
3. Finally, the gate driver sends a second pulse to turn the device back on. The current ramps up again, and the device is then turned off again

Figure 10. Typical double pulse setup and simplified waveforms



This sequence allows the extraction of all necessary information about the GaN devices, including switching times (rise time, fall time, delay times) and switching losses (energy loss during turn-on and turn off). In the following waveforms, we customized the double pulse test to a multipulse test to extract all parameters at different current levels, while avoiding self-heating of the die.

Let us compare the DP results among three different drive methods:

1. STGAP2GS with gate voltage between 0 V and +6.2 V - Figure 11
2. STGAP2GS with gate voltage between -3 V and +6.2 V
3. STDRIVEG611 with gate voltage between 0 V and + 6 V - Figure 12

Figure 11. **Multipulse with STGAP2GS - Positive voltage only**

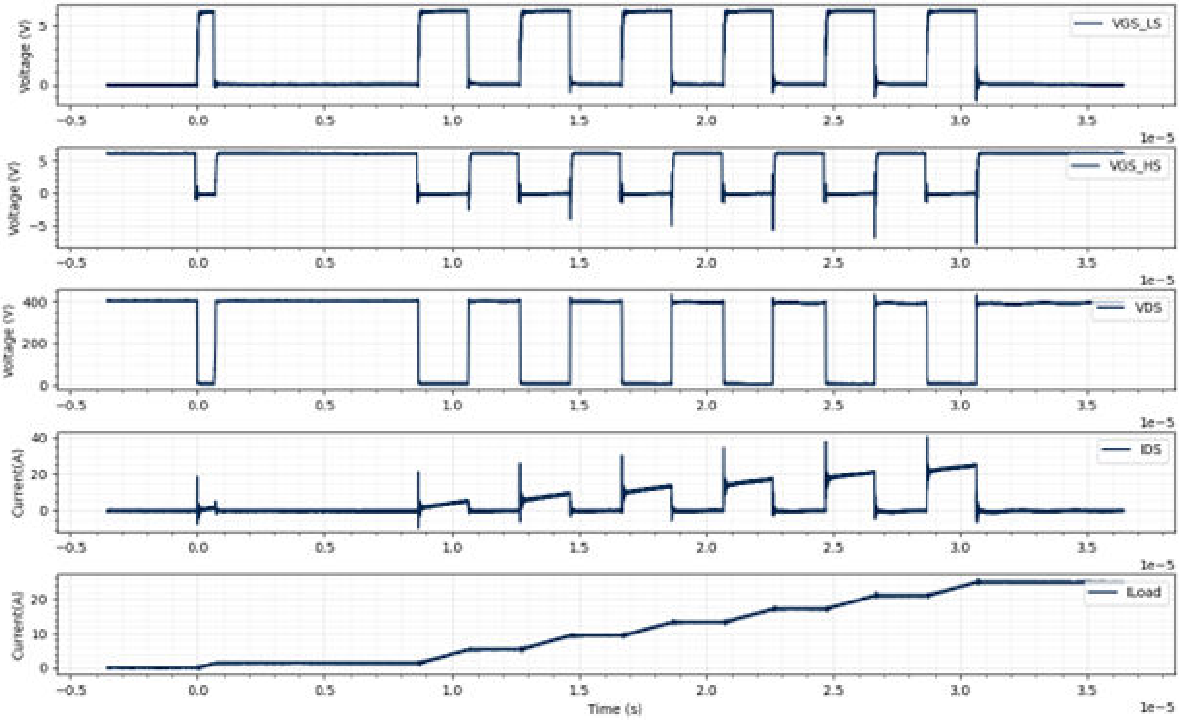
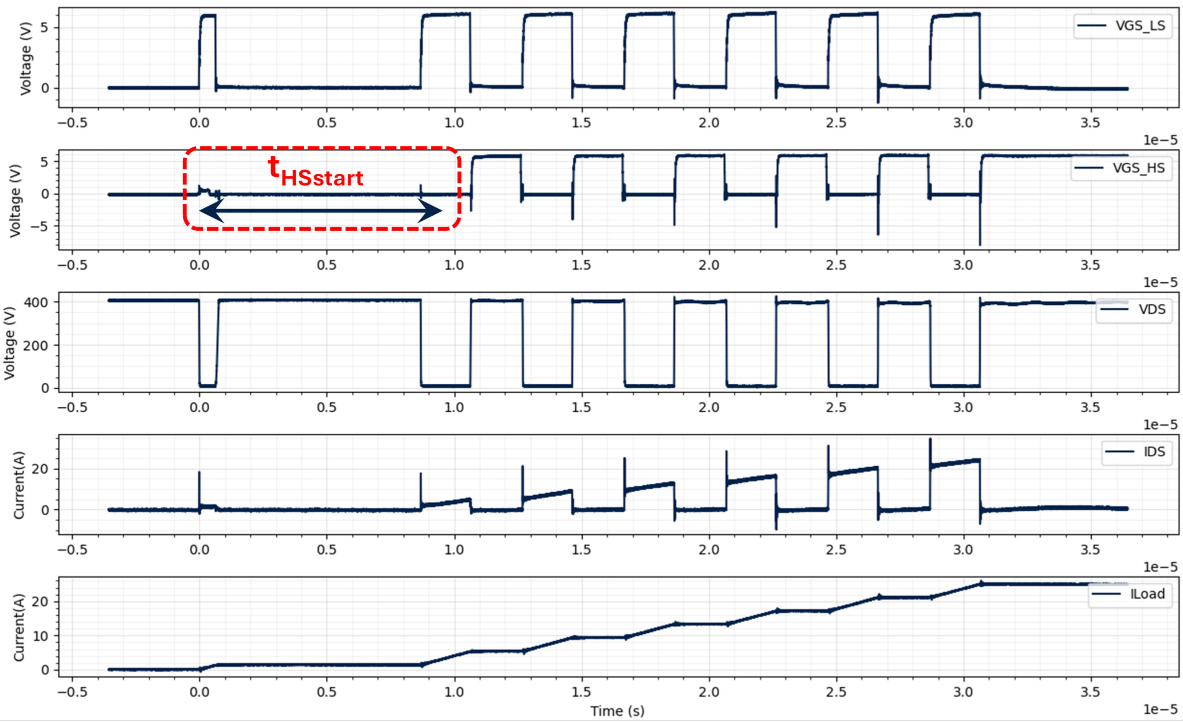


Figure 12. **Multipulse with STDRIVEG611**



One other particularity in the above procedure is related to the two first pulses. In the STDRIVEG611, a $t_{HSstart}$ timer (5 µs max) is implemented before accepting HS PWM signals to allow sufficient time for the bootstrap capacitor to be fully charged. To limit the effect of this particularity, a short pulse with a long off time is generated before producing the second pulse. In this case, only the first pulse operates asynchronously for the high-side switch. The same sequence has been applied to the STGAP2GS for a fair comparison.

Figure 13. Switching losses E_{ON} and E_{OFF}

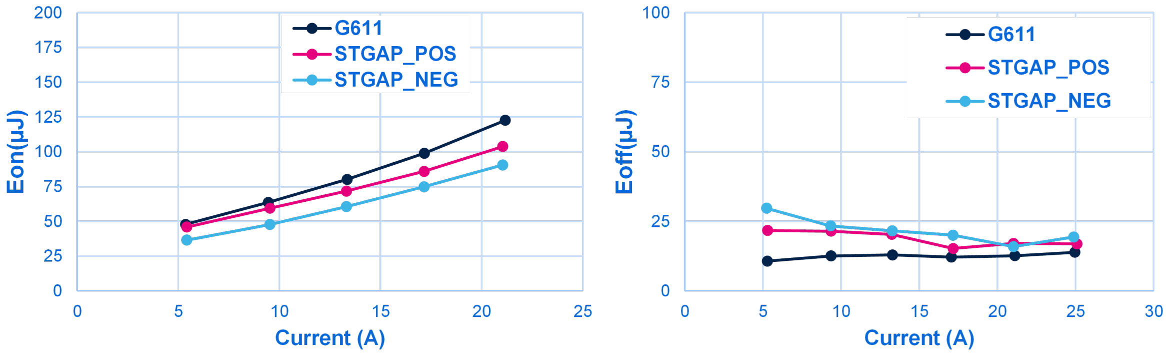


Figure 14. Rise and falling time

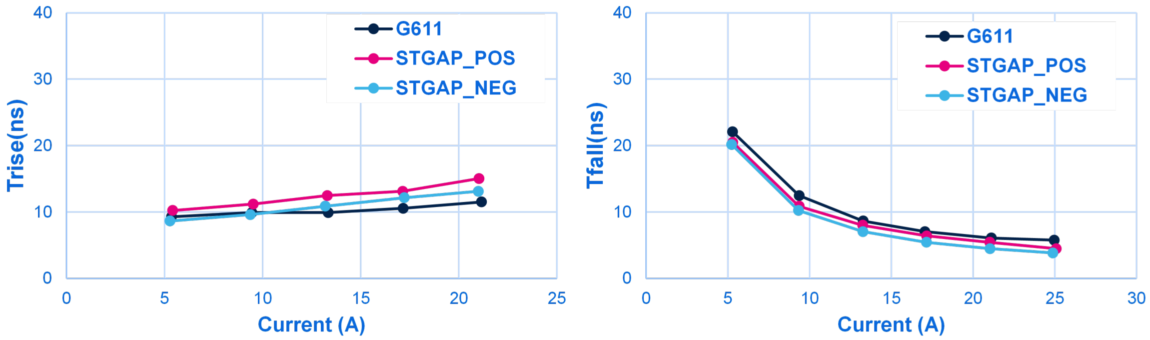
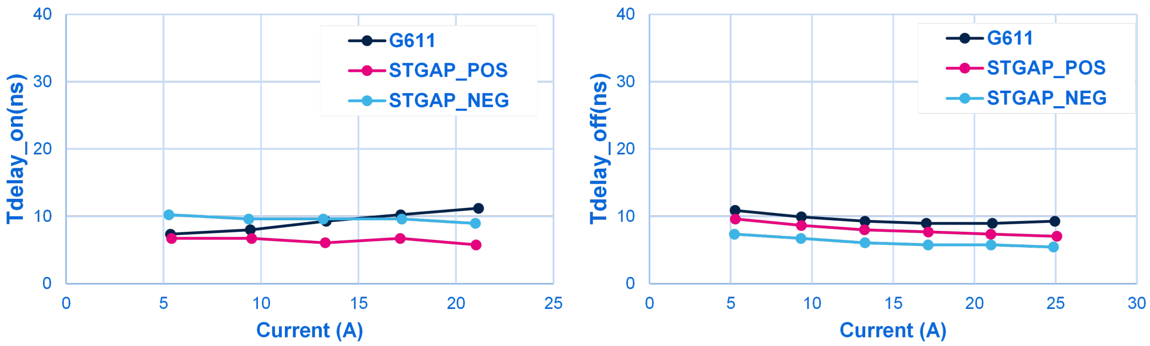
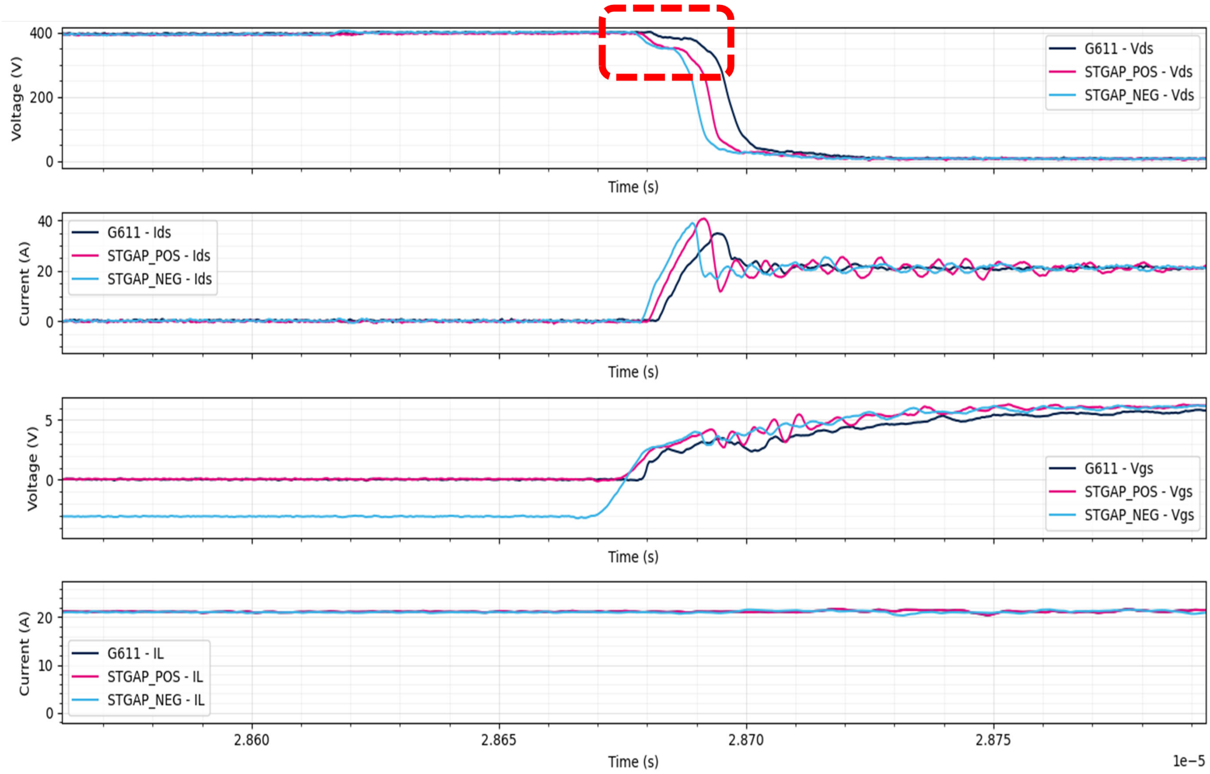


Figure 15. Delay time



From the above waveforms, all extracted parameters are very close to each other. At high current levels, we can notice a difference in the E_{ON} curve. A zoom-in has been done in to understand the reason.

Figure 16. E_{on} extraction at 21 A



With the STDRIVEG611 board, the plateau on the drain-to-source voltage during turn-on is larger and deeper compared to the STGAP2GS daughter board. This plateau is directly linked to the power loop and the corresponding parasitic inductance.

According to Figure 16, the parasitic inductance can be evaluated at 10 nH for the STGAP2GS daughter board and only 5.7 nH for the STDRIVEG611. We can also notice that the gate voltage is faster with the STGAP2GS.

Indeed, this isolated driver is stronger than the nonisolated one. The combination of these two elements leads to this difference.

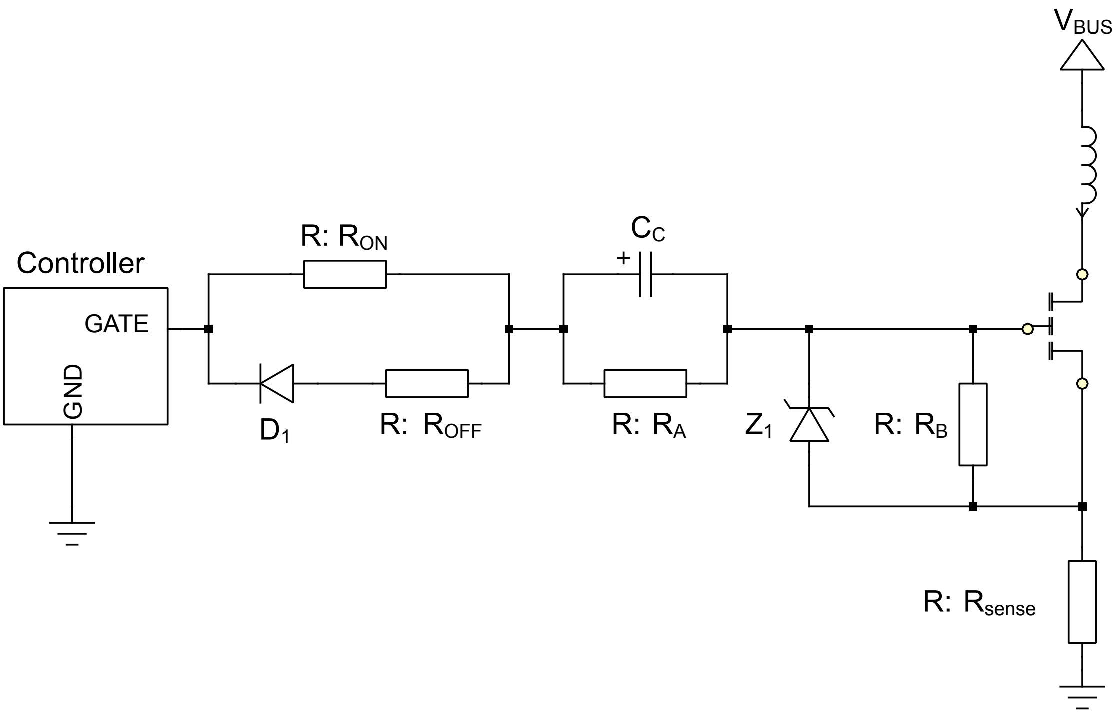
5 Driving GaN with MOSFET PWM controller

For some applications, the Power GaN needs to be driven by a MOSFET PWM controller that usually delivers a voltage higher that the maximum rating specified for a gate GaN device. A network with passive components can be inserted between the controller and the GaN transistor to shape the gate voltage.

As showed in the Figure 17, in addition to classical R_{ON}, R_{OFF} and diode D1, four passive components are needed:

- R_B: pull down the resistor
- R_A: to create a voltage divider
- Z_1: to clamp to the gate voltage
- C_C: switching acceleration capacitor

Figure 17. Voltage divider with limited negative voltage schematic



During turn-on, the driver current flows through the turn-on path (R_{ON}) and charges the device capacitances quickly. The presence of R_{ON} and C_C helps the gate voltage rise faster, which reduces turn-on delay and improves switching speed.

During turn-off, the gate capacitances discharge through the turn-off path (R_{OFF} + D_1). After the main capacitance discharge C_{ISS}, the remaining discharges of C_C force the gate voltage slightly negative with Z_1 and D_1 voltage drop that imposed the negative voltage threshold.

How to define a C_C capacitor?

The capacitor C_C is important because the divider resistance alone is too high impedance for fast switching. Since C_C has a low AC impedance, it supplies the switching current needed to charge and discharge the GaN capacitances C_{ISS} and C_{RSS}.

Design guidance for C_C:

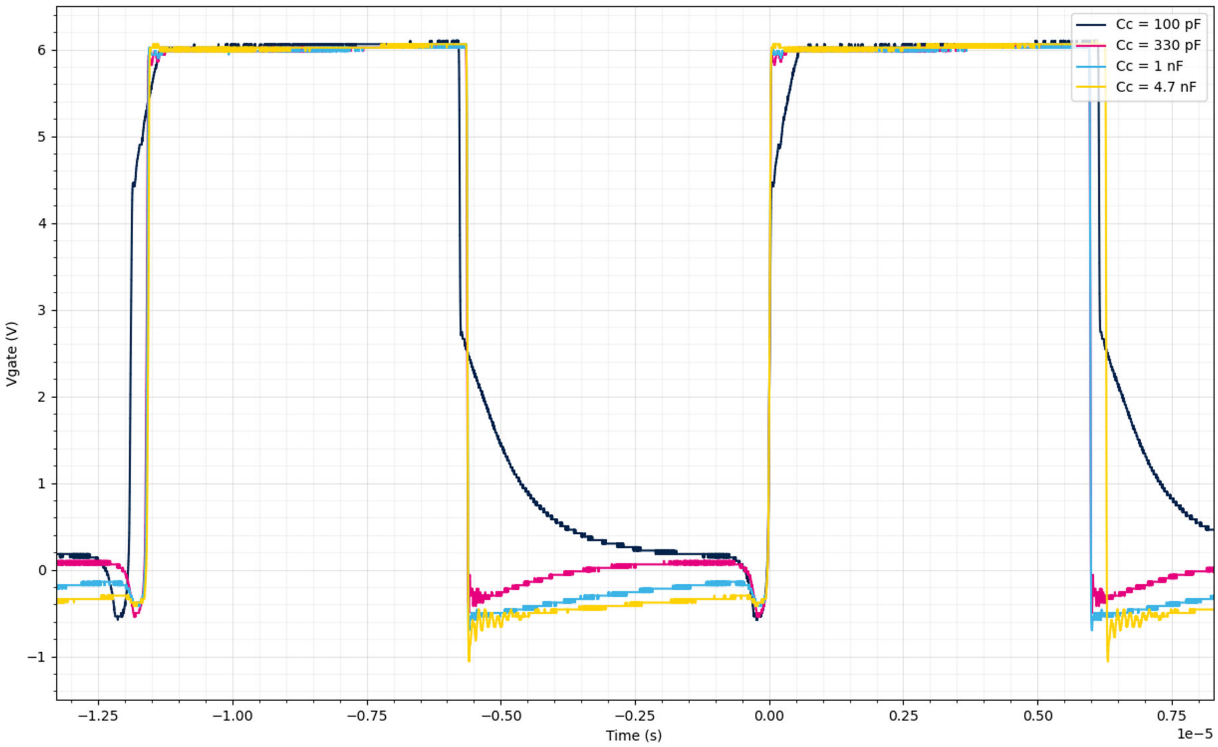
- If C_C is too small, switching becomes slow and the device may not fully switch in time
- If C_C is large enough, switching becomes faster
- If C_C is even larger, the negative gate voltage can be maintained during the all off-time duration

The first approach to determine a minimum value is:

$$C_C > \frac{Q_{GS} + Q_{GD}}{V_{\text{plateau}}} \quad (1)$$

Based on this result, taking a factor of four gives good results as shown in Figure 18 with a 4.7-nF capacitor for this GaN device. On the contrary, a 100 pF capacitor is not able to give the necessary energy to maintain a negative voltage.

Figure 18. Impact of Cc capacitor value with single Zener diode



How to define a resistor divider?

For Power GaN device, it is common to use a 10 kΩ pull-down resistance. This resistor ensures that the gate pin remains at 0 V and prevents unexpected turn-on when the controller is off or when a drive component fails or is unsoldered.

The resistance R_A can now be calculated considering several parameters:

- $V_{DRV(min)}$: minimum drive voltage delivered by the controller
- $V_{GS(ON)}$: on state gate voltage target
- V_{Rsense}: voltage drop across the sense resistance (usually at full load – OCP limit)
- $I_{GSS(max)}$: gate leakage current at 125 °C (worst case)

From the above parameters, R_A is equal to:

$$R_A = \frac{V_{\mathrm{DRV(min)}} - V_{\mathrm{GS(ON)}} - V_{\mathrm{Rsense}}}{\frac{V_{\mathrm{GS(ON)}}}{R_B} + I_{\mathrm{GSS(max)}}} \quad (2)$$

It should be $R_A + R_{ON}$ but R_{ON} is in the range of few ohms so negligible.

If we take an example to illustrate the above explanation. For a QR flyback tolopolgy, a 700-V GaN device is used with the characteristic related to the GaN and flyback application listed in the Table 1.

Table 1. Flyback and Power GaN characteristics

Reference	Values
Q_{GD}	0.66 nC
Q_{GS}	0.14 nC
$V_{plateau}$	2.1 V
$I_{GSS(max)}$ at125 °C	750 µA
$V_{GS(ON)}$	6.0 V
$V_{sense(max)}$	1.0 V
$V_{DRV(min)}$	8.55 V
R_B	10 kΩ

For this application, the capacitor C_C and resistor R_A can be computed:

$$C_C = \frac{0.14 \times 10^{-9} + 0.66 \times 10^{-9}}{2.1} = 380\mathrm{pF} \quad (3)$$

$$R_A = \frac{(8.55 - 6 - 1)}{\frac{6}{10k} + I_{\mathrm{GSS(max)}}} = 1.15\mathrm{k}\Omega \quad (4)$$

These values have to be confirmed and adjusted with experimental measurements.

Appendix A Acronyms and reference documents

Reference documents

[1] Datasheet *Galvanically isolated 3 A single gate driver for Enhancement mode GaN FETs* (DS14152)

[2] Datasheet *High voltage and high-speed half-bridge gate driver for GaN power switches* (DS14457)

[3] Data brief *Evaluation board for STDRIVEG611 600 V high-speed half-bridge gate driver with SGT120R65AL e-mode GaN HEMT* (DB5115).

[4] Data brief *Demonstration board for STGAP2GS galvanically isolated single gate driver with e-mode GaN transistor* (DB4955).

Revision history

Table 2. Document revision history

Date	Revision	Changes
28-Feb-2025	1	Initial release.
05-Aug-2026	2	Added Section 5: Driving GaN with MOSFET PWM controller. Updated Appendix A: Acronyms and reference documents.

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