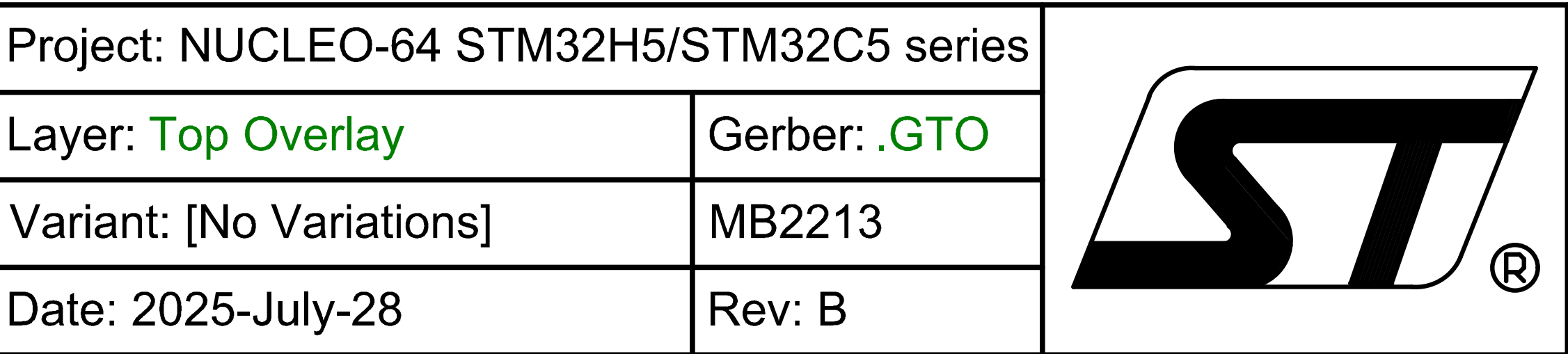
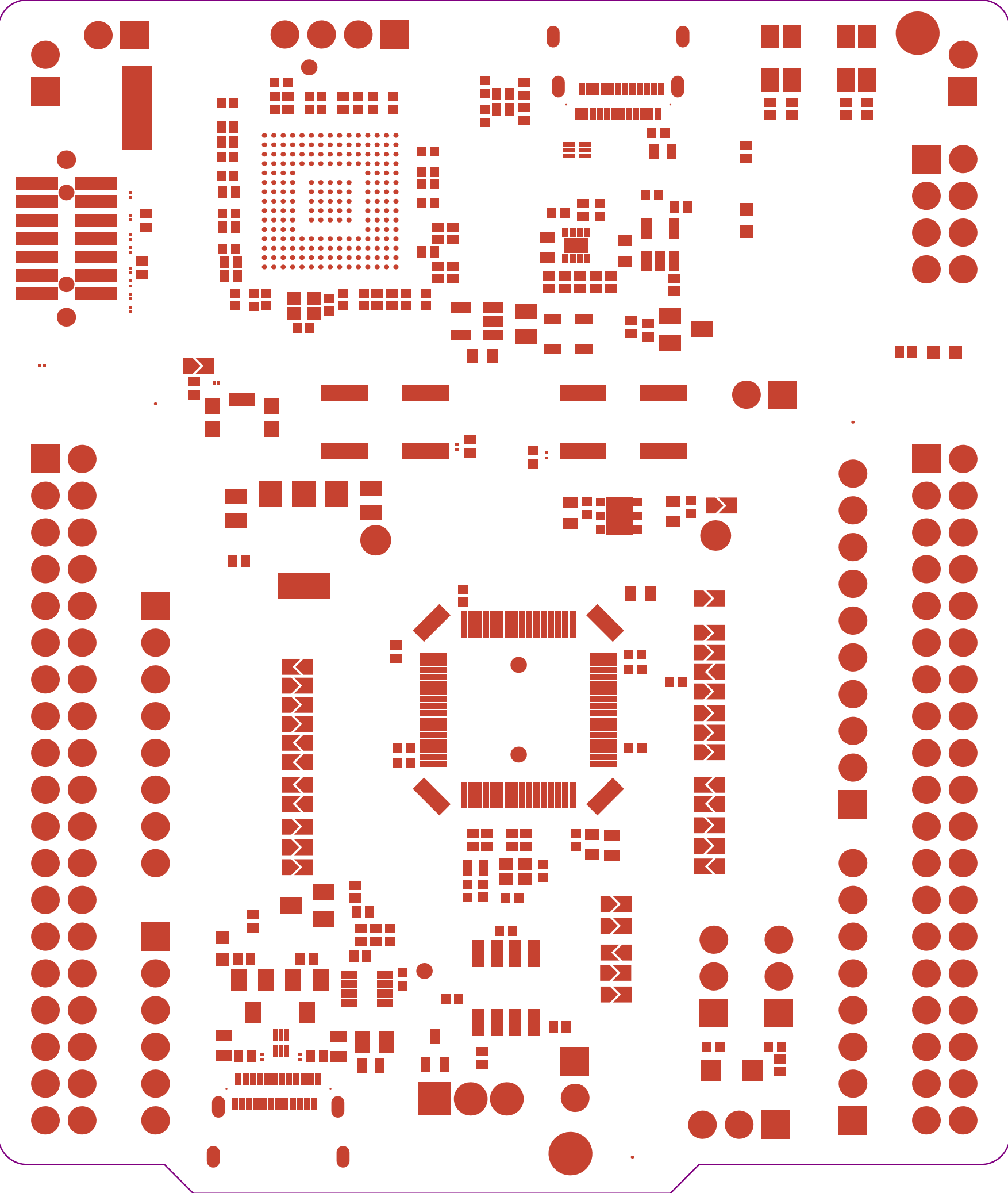
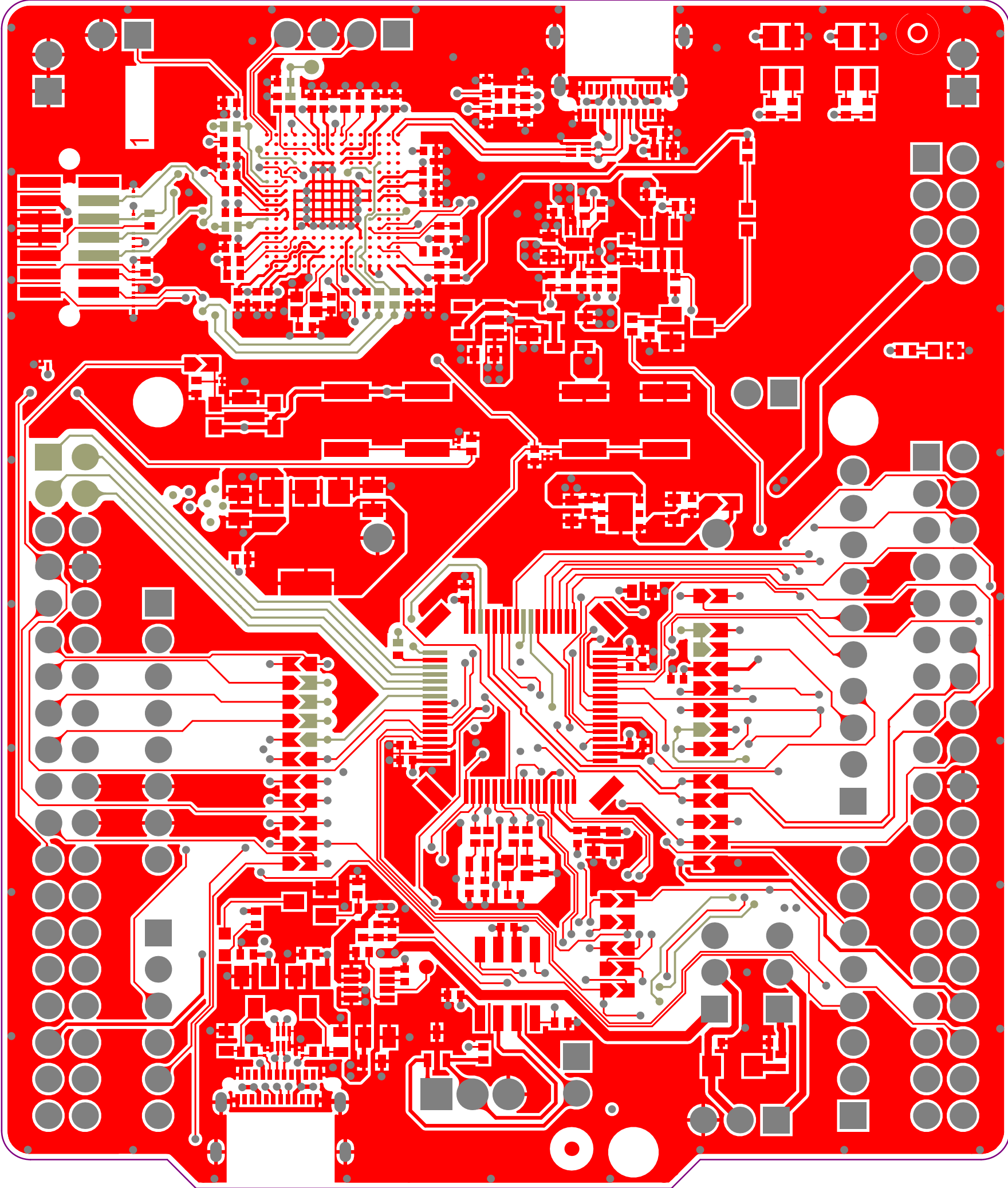


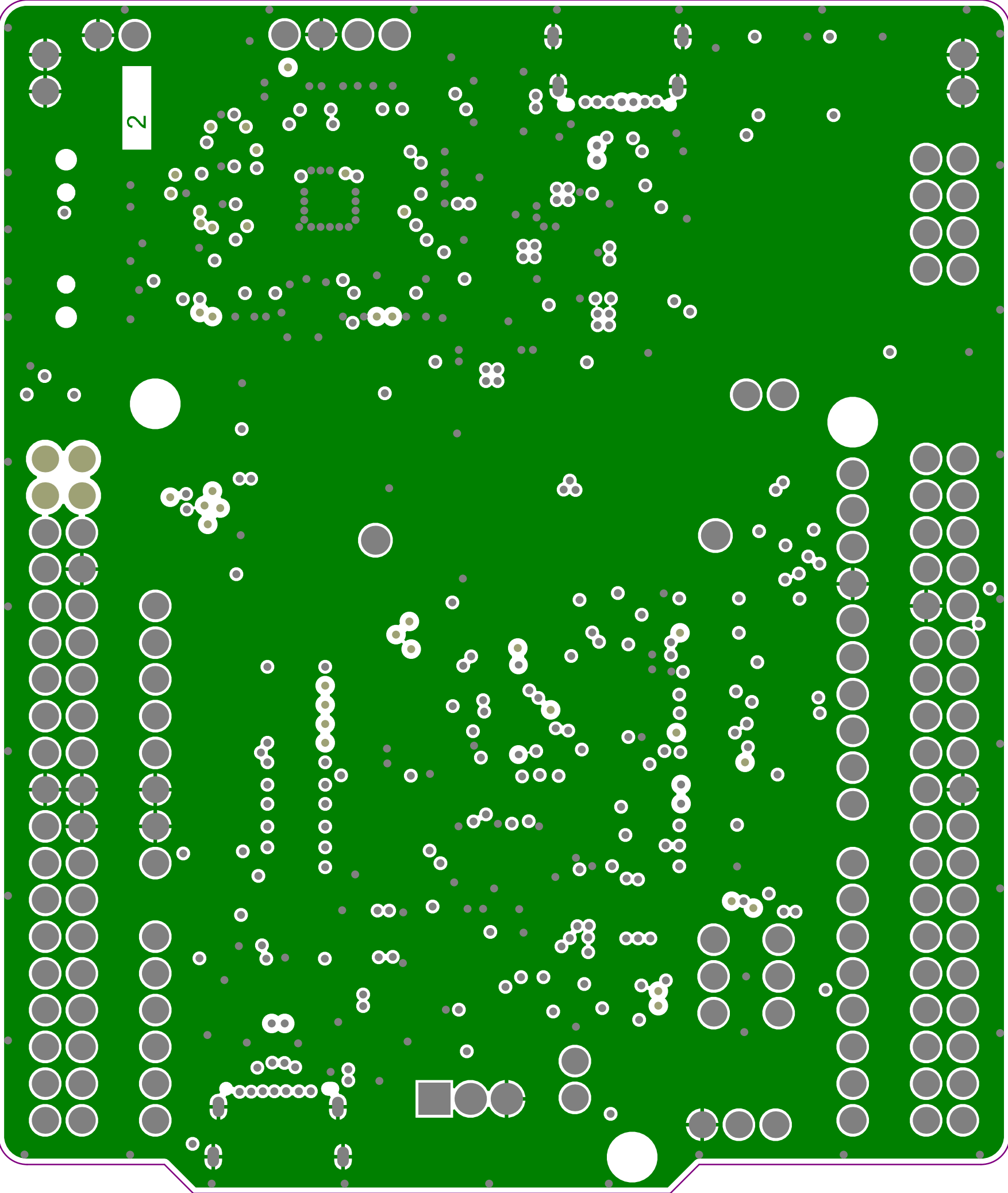




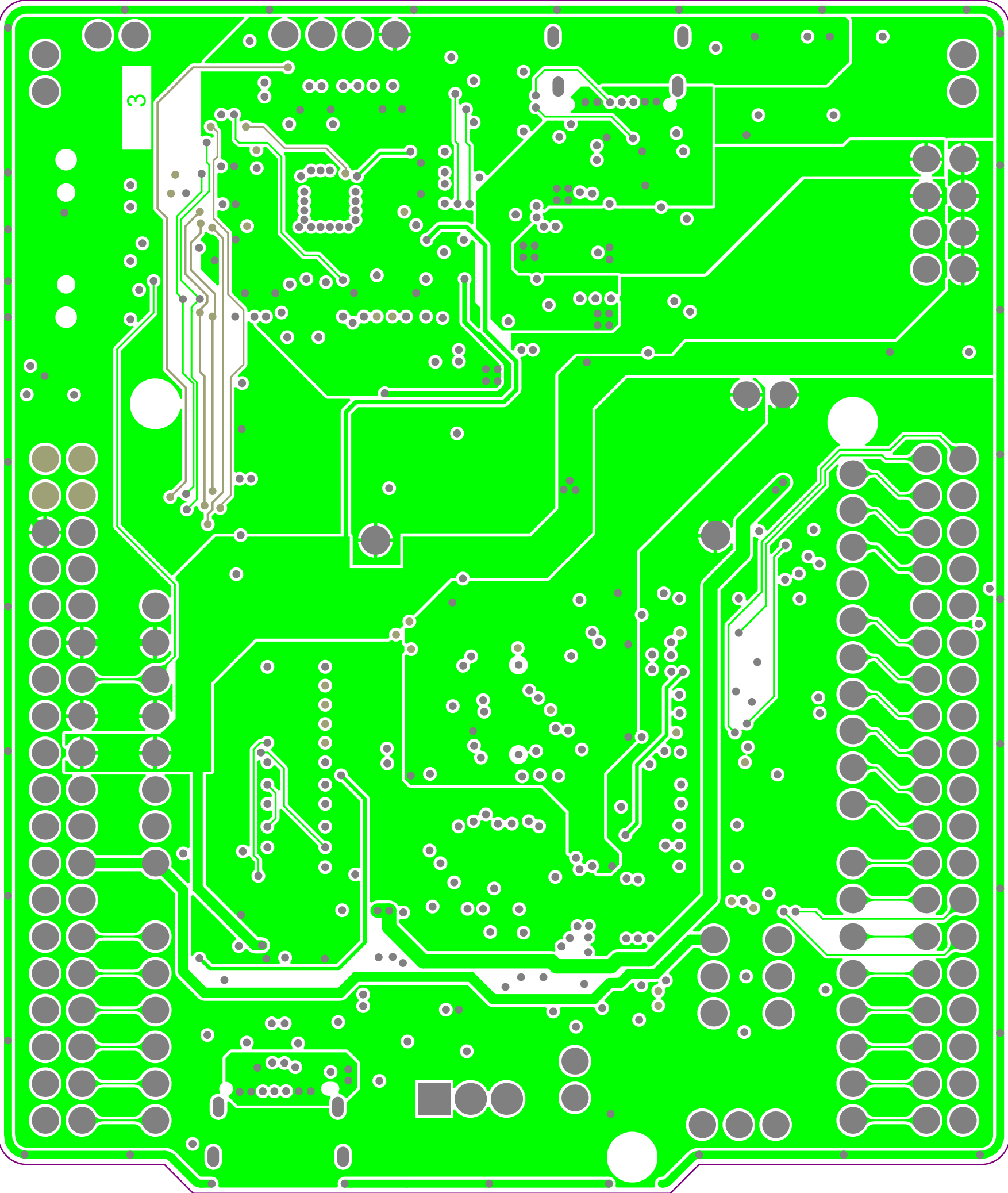
Project: NUCLEO-64 STM32H5/STM32C5 series		
Layer: Top Solder	Gerber: .GTS	
Variant: [No Variations]	MB2213	
Date: 2025-July-28	Rev: B	



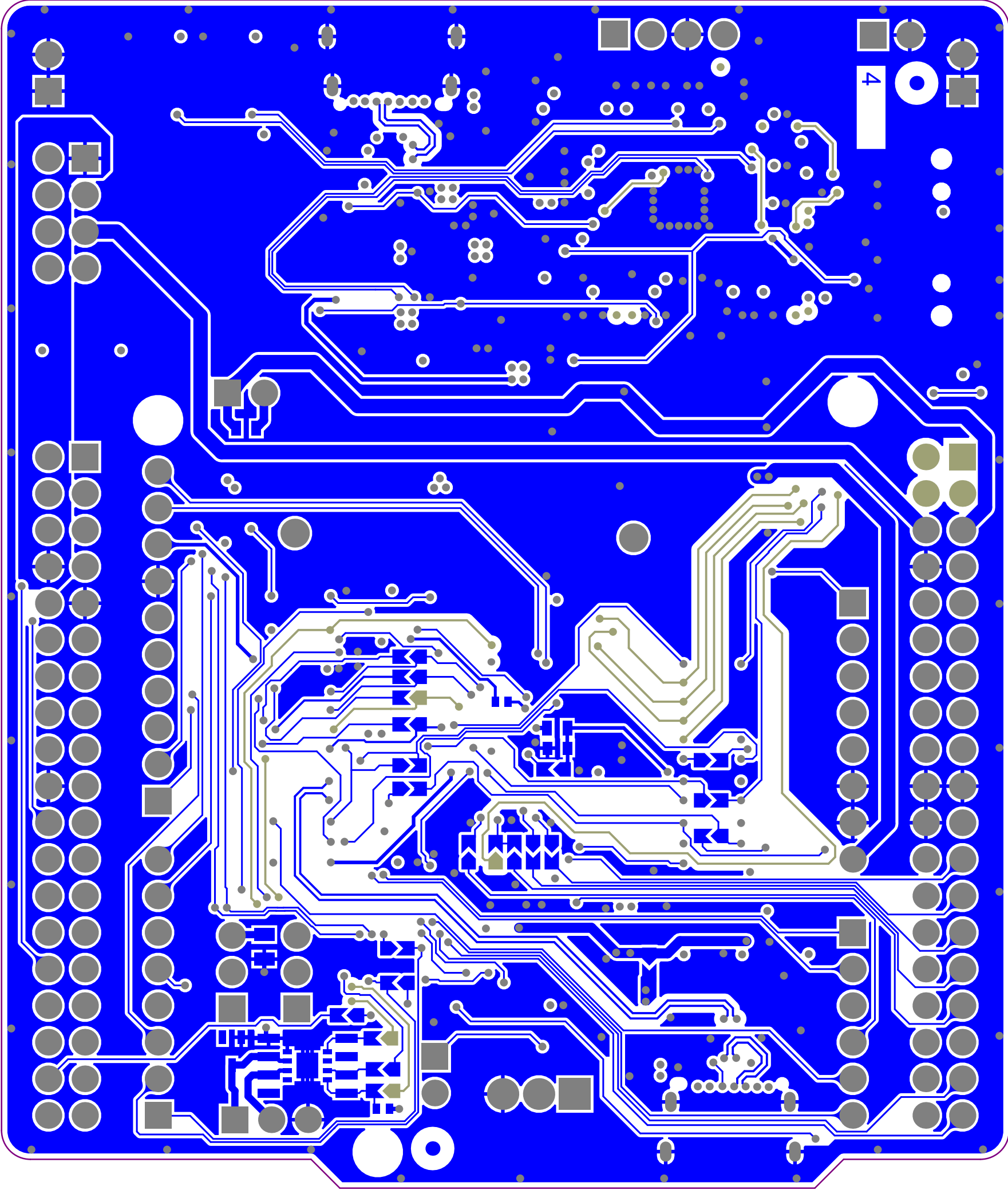
Project: NUCLEO-64 STM32H5/STM32C5 series		
Layer: Top Layer	Gerber: .GTL	
Variant: [No Variations]	MB2213	
Date: 2025-July-28	Rev: B	



Project: NUCLEO-64 STM32H5/STM32C5 series		
Layer: Signal Layer 1	Gerber: .G1	
Variant: [No Variations]	MB2213	
Date: 2025-July-28	Rev: B	



Project: NUCLEO-64 STM32H5/STM32C5 series		
Layer: Signal Layer 2	Gerber: .G2	
Variant: [No Variations]	MB2213	
Date: 2025-July-28	Rev: B	



Project: NUCLEO-64 STM32H5/STM32C5 series

Layer: Bottom Layer

Gerber: .GBL

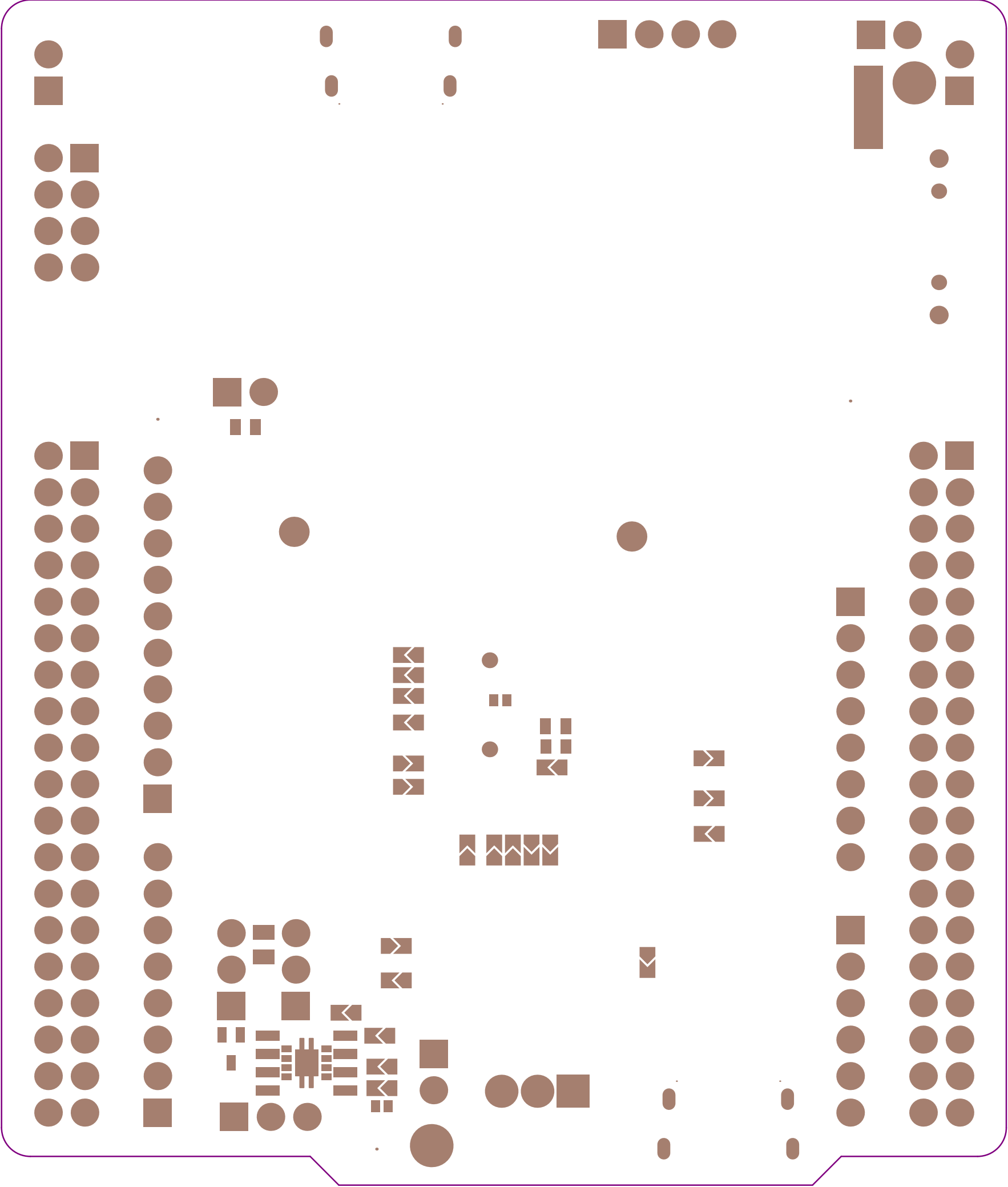
Variant: [No Variations]

MB2213

Date: 2025-July-28

Rev: B





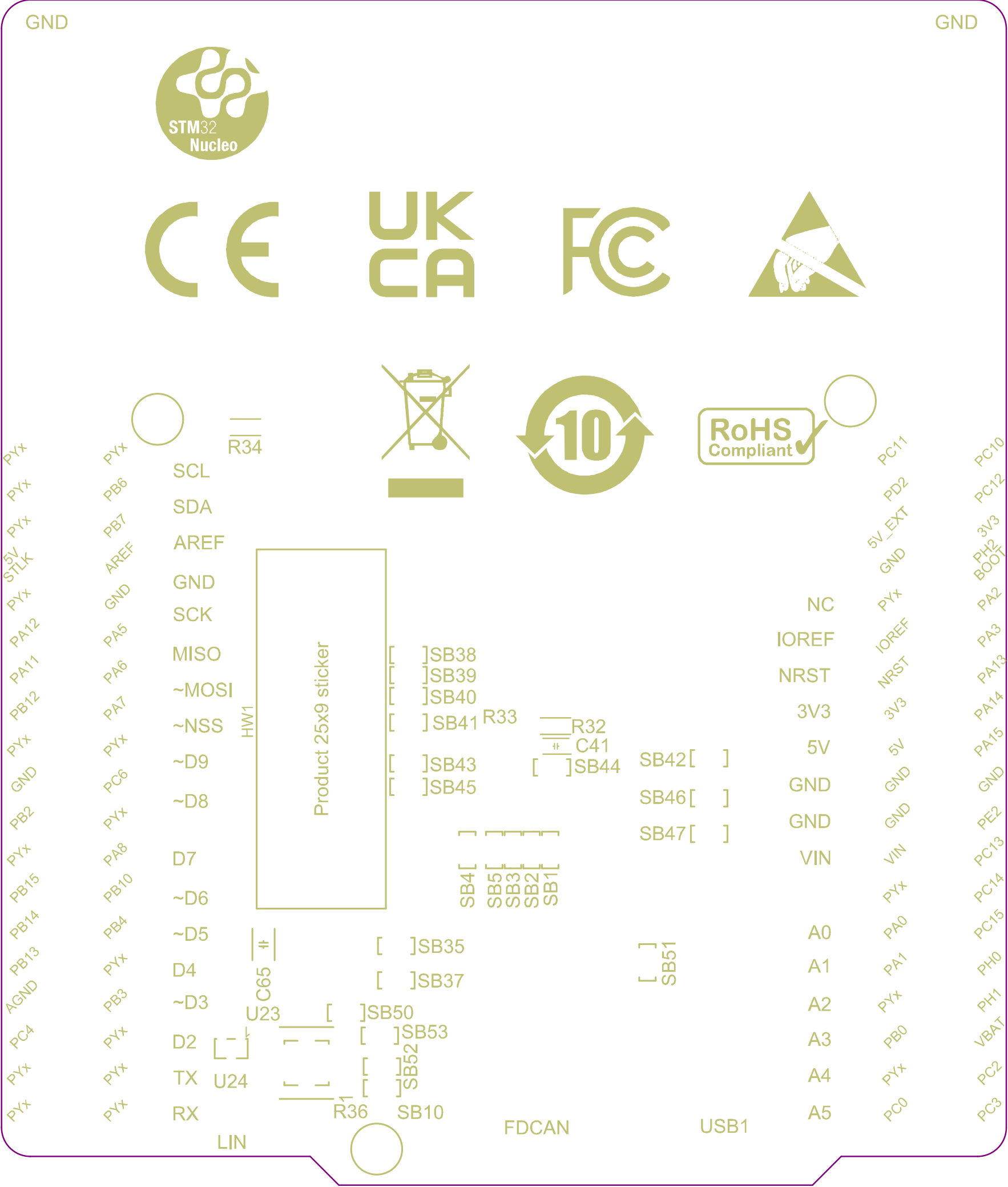
Project: NUCLEO-64 STM32H5/STM32C5 series

Layer: Board Layer Stack Bottom Gerber: .GBS

Variant: [No Variations] MB2213

Date: 2025-July-28 Rev: B





Project: NUCLEO-64 STM32H5/STM32C5 series

Layer: Board Layer Stack Bottom Gerber.GBO

Variant: [No Variations] MB2213

Date: 2025-July-28 Rev: B



THE COMPONENTS WITH PLATED THROUGH HOLE (PTH) MAY BE WELDED (CABLED) IN "PIN-IN-PASTE" MODE (IF NECESSARY)

PCB SPECIFICATIONS :

A. MATERIAL :

B. MATERIAL FAMILY :

C. SOLDERMASK COLOR :

D. SILKSCREEN COLOR :

E. SURFACE FINISH :

F. IMPEDANCE CONTROL :

G. THROUGH VIA :

H. STACK-UP :

FR-4

N/A

☐ GREEN

☐ WHITE

☐ ENIG

☐ HASL

☐ NO

☐ TG-170

☒ WHITE

☐ IMMERSION SILVER

☐ HASL (PB-FREE)

☒ YES (SEE IMPEDANCE TABLE FOR DETAIL INFORMATION)

☒ TG-150

☐ RED

☐ BLACK

☐ IMMERSION TIN

☐ GOLDEN FINGER

☐ TG-140

☒ Blue ink PANTONE 2955

☐ NON-CONDUCTIVE EPOXY.

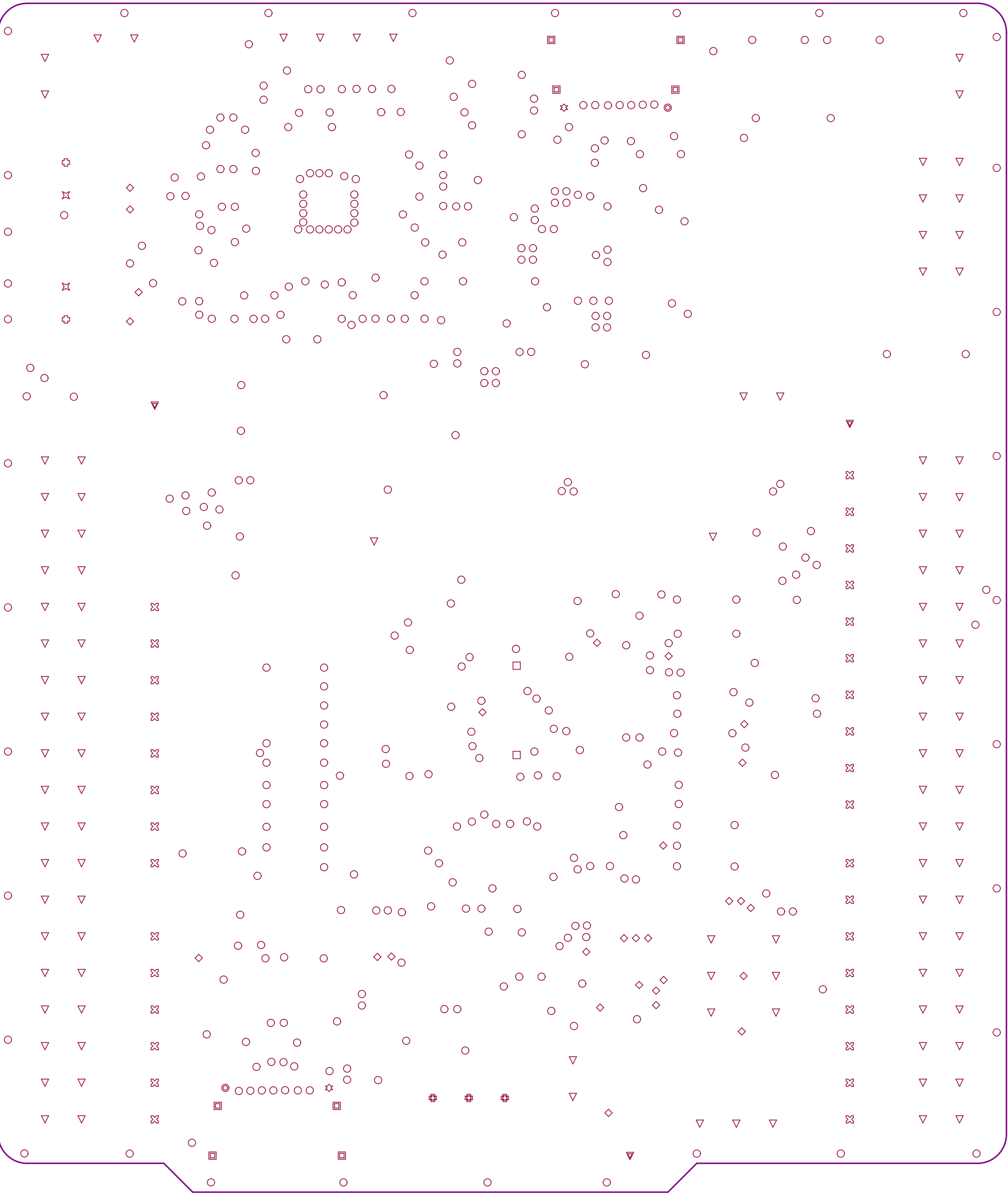
PLUG THE VIAS WHICH ARE COVERED WITH SOLDERMASK ONE OR TWO SIDE.
PLUG MATERIAL :
SEE LAYER STACK-UP SEQUENCE FOR OVERALL THICKNESS.

PCB : TYPE 3

ASPECT-RATIO, AXE Z :
6:1 to 8:1
LEVEL "B"

MINIMUM PARAMETERS

DEFAULT
TRACKS : 0.120mm
GAPS : 0.120mm



Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
	Top Overlay					
	Top Solder	Solder Resist	0.015mm	3.5		
1	Top Layer		0.035mm			
	Dielectric 1	FR-4	0.096mm	3.8		
2	Signal Layer 1		0.035mm			
	Dielectric 2	FR-4	1.300mm	5.1		
3	Signal Layer 2		0.035mm			
	Dielectric 3	FR-4	0.096mm	3.8		
4	Bottom Layer		0.035mm			
	Board Layer Stack Bottom Solder	Solder Resist	0.015mm	3.5		
	Board Layer Stack Bottom Overlay					

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
◇	28	0.30mm (11.81mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v55h30m0mx0
○	427	0.35mm (13.78mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v55h35m0mx0
▣	8	0.50mm (19.69mil)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	r140_80h50_110r40m150_90
⊙	2	0.65mm (25.59mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c0hn65m10
✱	2	0.65mm (25.59mil)	NPTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	c0hn65_95m10
✱	2	0.97mm (38.19mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c0hn97m107
□	2	1.00mm (39.37mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c50hn100m110
▽	109	1.00mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)
✕	32	1.10mm (43.31mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)
⊕	2	1.19mm (46.85mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c0hn119m129
⊕	3	1.40mm (55.12mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
▽	3	3.20mm (125.98mil)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c0hn320m20
	620 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Project: NUCLEO-64 STM32H5/STM32C5 series

Layer: Drill Drawing

Variant: [No Variations]

Date: 2025-July-28

Gerber: .DRL

MB2213

Rev: B