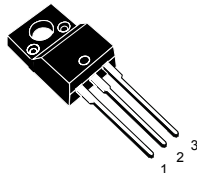
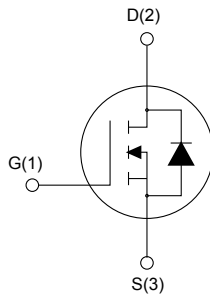


N-channel 500 V, 400 mΩ typ., 8.5 A MDmesh II Power MOSFET in a TO-220FP package



TO-220FP



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Product status link
[STF11NM50N](#)
Product summary

Order code	STF11NM50N
Marking	11NM50N
Package	TO-220FP
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF11NM50N	500 V	470 mΩ	8.5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	8.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	34	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	25	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 8.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	5	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	500	-	-	V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 500 V	-	-	1	μA
		V _{GS} = 0 V, V _{DS} = 500 V, T _C = 125 °C ⁽¹⁾	-	-	100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V	-	-	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 4.5 A	-	400	470	mΩ

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	547	-	pF
C _{oss}	Output capacitance		-	42	-	pF
C _{rss}	Reverse transfer capacitance		-	2	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 400 V, V _{GS} = 0 V	-	210	-	pF
R _g	Gate input resistance	f = 1 MHz, I _D = 0 A	-	5.8	-	Ω
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 8.5 A, V _{GS} = 0 to 10 V (see the Figure 13. Test circuit for gate charge behavior)	-	19	-	nC
Q _{gs}	Gate-source charge		-	3.7	-	nC
Q _{gd}	Gate-drain charge		-	10	-	nC

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 250 V, I _D = 4.25 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	8	-	ns
t _r	Rise time		-	10	-	ns
t _{d(off)}	Turn-off delay time	(see the Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	33	-	ns
t _f	Fall time		-	10	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	8.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	34	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$	-	230	-	ns
Q_{rr}	Reverse recovery charge		-	2.1	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	18	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	275	-	ns
Q_{rr}	Reverse recovery charge		-	2.5	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	18	-	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

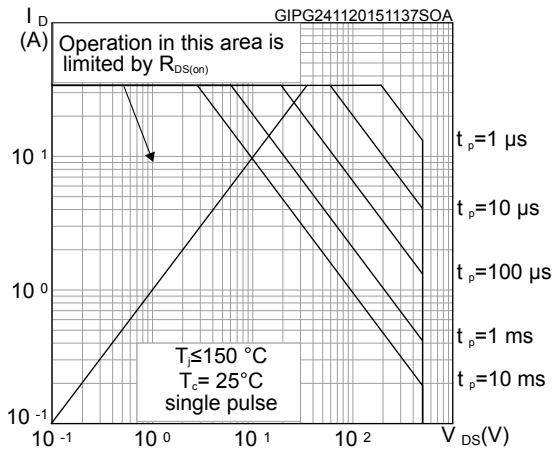
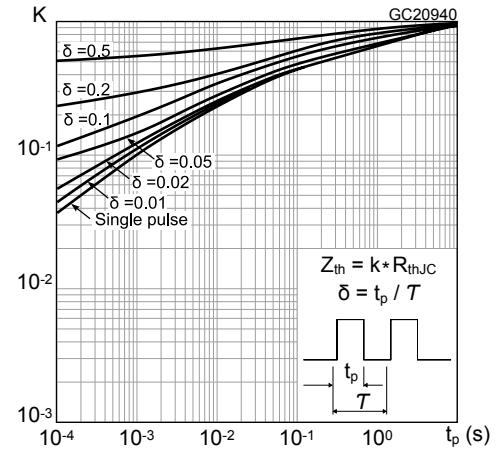
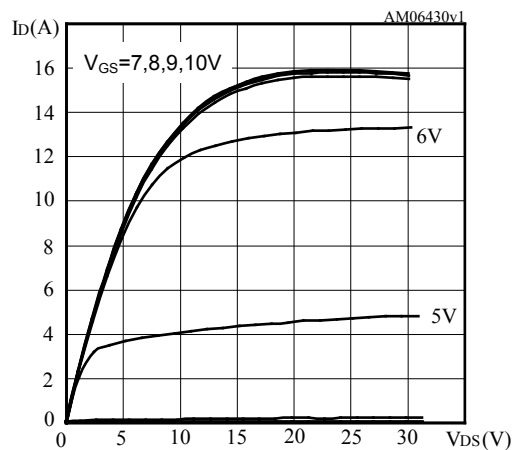
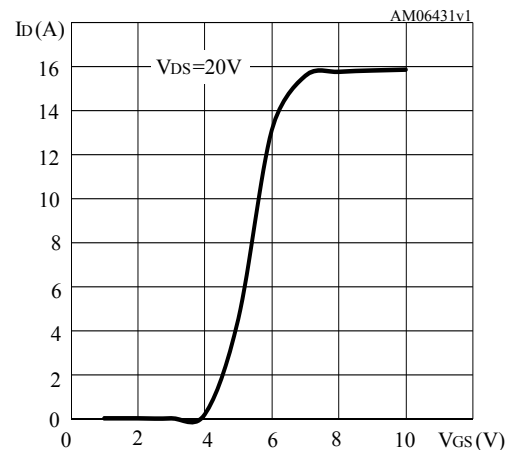
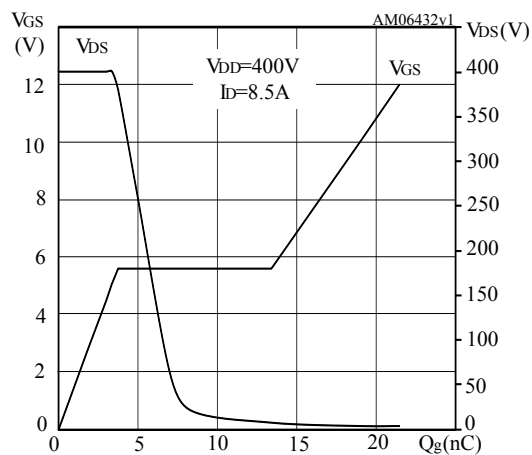
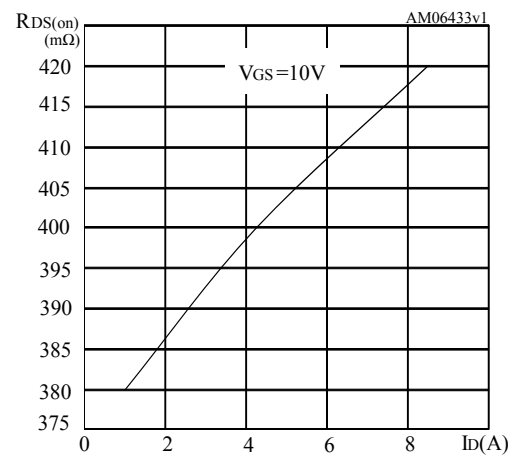
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

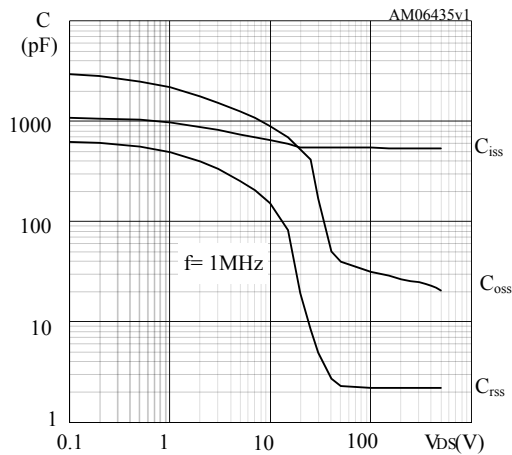


Figure 8. Typical output capacitance stored energy

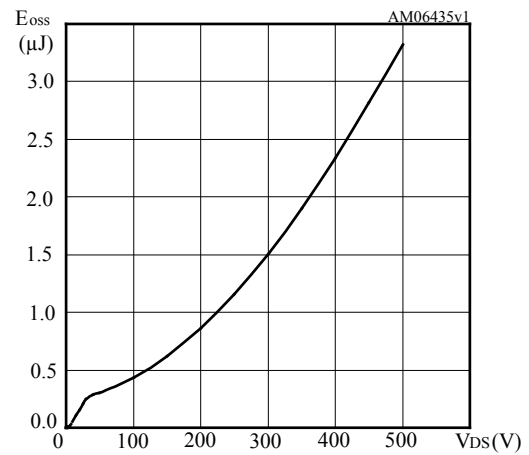


Figure 9. Normalized gate threshold vs temperature

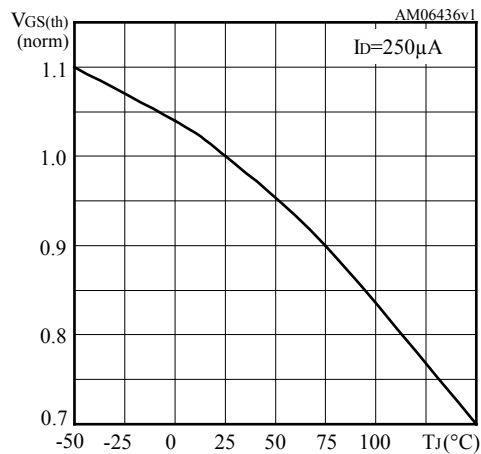


Figure 10. Normalized on-resistance vs temperature

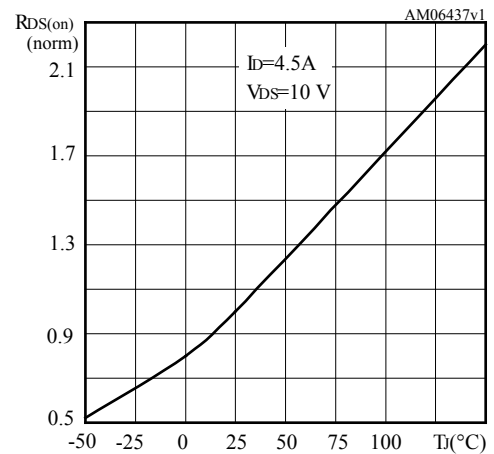
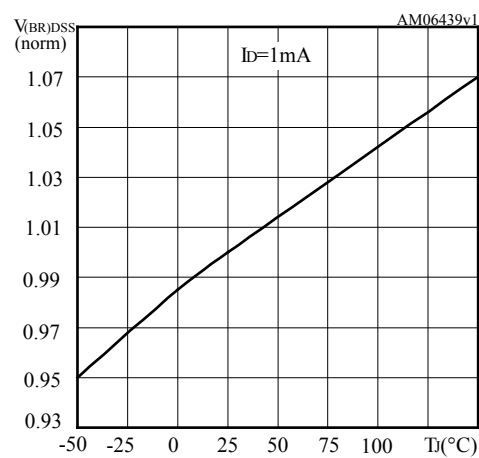


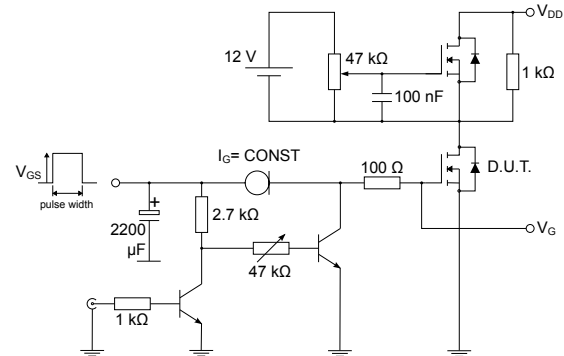
Figure 11. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 12. Test circuit for resistive load switching times


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Figure 13. Test circuit for gate charge behavior


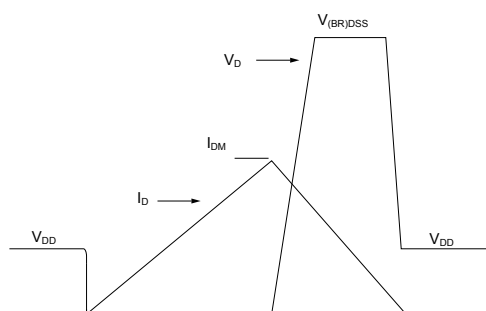
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Figure 14. Test circuit for inductive load switching and diode recovery times


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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform

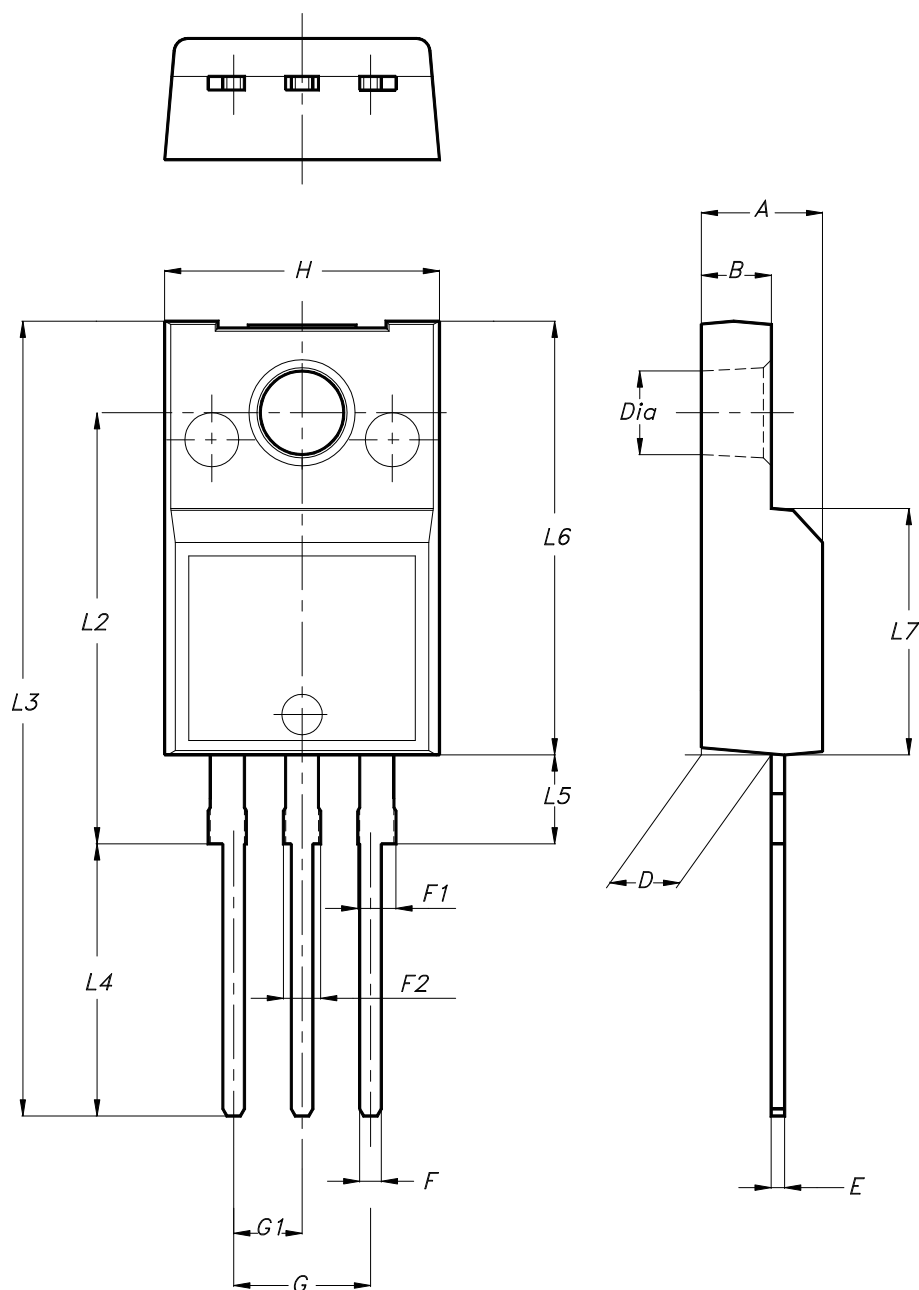

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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 18. TO-220FP type B package outline



7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. Document revision history

Date	Version	Changes
25-Nov-2015	1	First release. Part number previously included in datasheet DocID17156.
09-Jun-2016	2	Updated I_{GSS} unit from μA to nA in <i>Table 5: "On/off states"</i> . Updated <i>Table 7: "Switching times"</i> modifying references in test conditions. Document reformatted with the current standard with minor text changes to improve readability.
23-Apr-2026	3	Updated Section 4: Package information . Minor text changes.

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