

## Galvanically isolated 4 A single gate driver



SO-8W



Product status link

[STGAP2HS](#)

Product label



### Features

- Driver current capability: 4 A sink/source @25°C
- 100 V/ns Common Mode Transient Immunity (CMTI)
- Overall input-output propagation delay: 75 ns
- Separate sink and source option for easy gate driving configuration
- 4 A Miller CLAMP dedicated pin option
- UVLO function
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shut-down protection
- Standby function
- Wide body SO-8W package
- Galvanic isolation IEC 60747-17 certified, UL 1577 recognized
  - Maximum Repetitive Isolation Voltage  $V_{IORM} = 1.2 \text{ kV}_{PEAK}$
  - Transient Overvoltage  $V_{IOTM} = 5.0 \text{ kV}_{PEAK}$
  - Isolation voltage  $V_{ISO} = 3.5 \text{ kV}_{RMS}$

### Application

- Motor driver for home appliances, factory automation, industrial drives and fans.
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

### Description

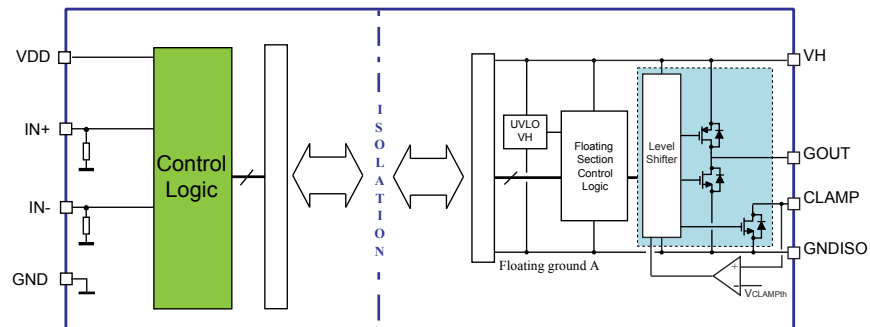
The **STGAP2HS** is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for mid and high power applications such as power conversion and motor driver inverters in industrial applications. The device is available in two different configurations. The configuration with separated output pins allows to independently optimize turn-on and turn-off by using dedicated gate resistors. The configuration featuring single output pin and Miller CLAMP function prevents gate spikes during fast commutations in half-bridge topologies. Both configurations provide high flexibility and bill of material reduction for external components.

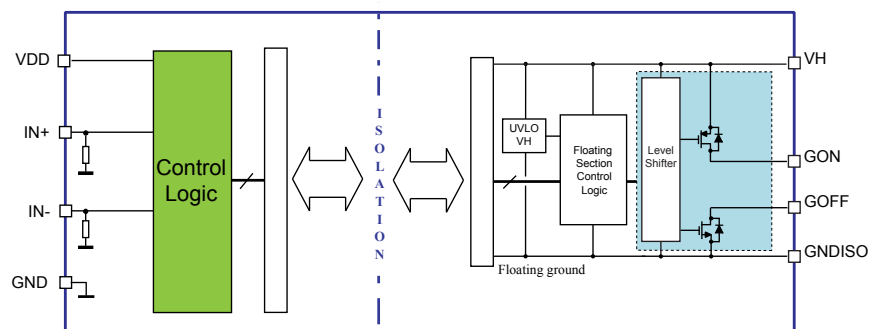
The device integrates UVLO and thermal shutdown protection functions to facilitate the design of highly reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction. The input to output propagation delay is less than 75 ns, which delivers high PWM control accuracy. A standby mode is available to reduce idle power consumption.

# 1 Block diagram

**Figure 1. Block diagram - Single output and Miller Clamp configuration**

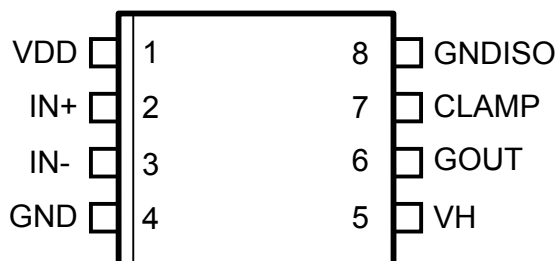


**Figure 2. Block diagram - Separate output configuration**

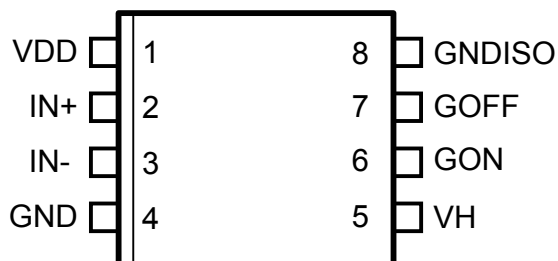


## 2 Pin description and connection diagram

**Figure 3. Pin connection (top view) - Single output and Miller CLAMP option**



**Figure 4. Pin connection (top view) - Separated outputs option**



**Table 1. Pin Description**

| Pin #    |          | Pin Name | Type          | Function                              |
|----------|----------|----------|---------------|---------------------------------------|
| Figure 4 | Figure 3 |          |               |                                       |
| 1        | 1        | VDD      | Power Supply  | Driver logic supply voltage.          |
| 2        | 2        | IN+      | Logic Input   | Driver logic input, active high.      |
| 3        | 3        | IN-      | Logic Input   | Driver logic input, active low.       |
| 4        | 4        | GND      | Power Supply  | Driver logic ground.                  |
| 5        | 5        | VH       | Power Supply  | Gate driving positive voltage supply. |
| -        | 6        | GOUT     | Analog Output | Sink/Source output.                   |
| -        | 7        | CLAMP    | Analog Output | Active Miller Clamp.                  |
| 6        | -        | GON      | Analog Output | Source output.                        |
| 7        | -        | GOFF     | Analog Output | Sink output.                          |
| 8        | 8        | GNDISO   | Power Supply  | Gate driving Isolated ground.         |

## 3 Electrical data

### 3.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter                                                    | Test condition | Min. | Max.   | Unit |
|--------------------|--------------------------------------------------------------|----------------|------|--------|------|
| VDD                | Logic supply voltage vs. GND                                 | -              | -0.3 | 6.5    | V    |
| V <sub>LOGIC</sub> | Logic pins voltage vs. GND                                   | -              | -0.3 | 6.5    | V    |
| VH                 | Positive supply voltage (VH vs. GNDISO)                      | -              | -0.3 | 28     | V    |
| V <sub>OUT</sub>   | Voltage on gate driver outputs (GON, GOFF, CLAMP VS. GNDISO) | -              | -0.3 | VH+0.3 | V    |
| T <sub>J</sub>     | Junction temperature                                         | -              | -40  | 150    | °C   |
| T <sub>stg</sub>   | Storage temperature                                          | -              | -50  | 150    | °C   |
| ESD                | HBM (human body model)                                       | -              | 2    |        | kV   |

### 3.2 Recommended operating conditions

**Table 3. Recommended operating conditions**

| Symbol             | Parameter                                  | Test conditions | Min.                   | Max. | Unit |
|--------------------|--------------------------------------------|-----------------|------------------------|------|------|
| VDD                | Logic supply voltage vs. GND               | -               | 3.1                    | 5.5  | V    |
| V <sub>LOGIC</sub> | Logic pins voltage vs. GND                 | -               | 0                      | 5.5  | V    |
| VH                 | Positive supply voltage (VH vs. GNDISO)    | -               | Max(VH <sub>ON</sub> ) | 26   | V    |
| F <sub>SW</sub>    | Maximum switching frequency <sup>(1)</sup> | -               | -                      | 1    | MHz  |
| t <sub>OUT</sub>   | Output pulse width (GOUT, GON-GOFF)        | -               | 100                    | -    | ns   |
| T <sub>J</sub>     | Operating junction temperature             | -               | -40                    | 125  | °C   |
| T <sub>amb</sub>   | Ambient temperature                        | -               | -40                    | 125  | °C   |

1. Actual limit depends on power dissipation and T<sub>J</sub>.

### 3.3 Thermal data

**Table 4. Thermal data**

| Symbol              | Parameter                              | Package | Value | Unit |
|---------------------|----------------------------------------|---------|-------|------|
| R <sub>th(JA)</sub> | Thermal resistance junction to ambient | SO-8W   | 120   | °C/W |

## 4 Electrical characteristics

Testing conditions:  $T_J = 25^\circ\text{C}$ ,  $V_H = 15\text{ V}$ ,  $V_{DD} = 5\text{ V}$  unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol                         | Pin      | Parameter                                        | Test conditions                                         | Min.                | Typ.                | Max.                | Unit          |
|--------------------------------|----------|--------------------------------------------------|---------------------------------------------------------|---------------------|---------------------|---------------------|---------------|
| <b>Dynamic characteristics</b> |          |                                                  |                                                         |                     |                     |                     |               |
| $t_{Don}$                      | IN+, IN- | Input to output propagation delay ON             | -                                                       | 50                  | 75                  | 90                  | ns            |
| $t_{Doff}$                     | IN+, IN- | Input to output propagation delay OFF            | -                                                       | 50                  | 75                  | 90                  | ns            |
| $t_r$                          | -        | Rise time                                        | CL = 4.7 nF<br>See Figure 16                            | -                   | 30                  | -                   | ns            |
| $t_f$                          | -        | Fall time                                        |                                                         | -                   | 30                  | -                   | ns            |
| PWD                            | -        | Pulse Width Distortion<br>$ t_{Don} - t_{Doff} $ | -                                                       | -                   | -                   | 20                  | ns            |
| $t_{deglitch}$                 | IN+, IN- | Inputs deglitch filter                           | -                                                       | -                   | 20                  | 40                  | ns            |
| CMTI <sup>(1)</sup>            | -        | Common-mode transient immunity, $ dV_{ISO}/dt $  | $V_{CM} = 1500\text{ V}$ ,<br>See Figure 15             | 100                 | -                   | -                   | V/ns          |
| <b>Supply voltage</b>          |          |                                                  |                                                         |                     |                     |                     |               |
| $V_{H_{on}}$                   | -        | VH UVLO turn-on threshold                        | -                                                       | 8.6                 | 9.1                 | 9.6                 | V             |
| $V_{H_{off}}$                  | -        | VH UVLO turn-off threshold                       | -                                                       | 7.9                 | 8.4                 | 8.9                 | V             |
| $V_{H_{hyst}}$                 | -        | VH UVLO hysteresis                               | -                                                       | 600                 | 750                 | 950                 | mV            |
| $I_{QHU}$                      | -        | VH undervoltage quiescent supply current         | $V_H = 7\text{ V}$                                      | -                   | 1.3                 | 1.8                 | mA            |
| $I_{QH}$                       | -        | VH quiescent supply current                      | -                                                       | -                   | 1.3                 | 1.8                 | mA            |
| $I_{QH_{SBY}}$                 | -        | Standby VH quiescent supply current              | Standby mode                                            | -                   | 400                 | 550                 | $\mu\text{A}$ |
| SafeClp                        | -        | GOFF active clamp                                | $I_{GOFF} = 0.2\text{ A}$ ;<br>VH floating              | -                   | 2                   | 2.3                 | V             |
| $I_{QDD}$                      | -        | VDD quiescent supply current                     | -                                                       | -                   | 1.0                 | 1.3                 | mA            |
| $I_{QDD_{SBY}}$                | -        | Standby VDD quiescent supply current             | Standby mode                                            | -                   | 40                  | 65                  | $\mu\text{A}$ |
| <b>Logic Inputs</b>            |          |                                                  |                                                         |                     |                     |                     |               |
| $V_{il}$                       | IN+, IN- | Low level logic threshold voltage                | -                                                       | $0.29 \cdot V_{DD}$ | $0.33 \cdot V_{DD}$ | $0.37 \cdot V_{DD}$ | V             |
| $V_{ih}$                       | IN+, IN- | High level logic threshold voltage               | -                                                       | $0.62 \cdot V_{DD}$ | $0.66 \cdot V_{DD}$ | $0.70 \cdot V_{DD}$ | V             |
| $I_{INh}$                      | IN+, IN- | INx logic "1" input bias current                 | $IN_x = 5\text{ V}$                                     | 33                  | 50                  | 70                  | $\mu\text{A}$ |
| $I_{INl}$                      | IN+, IN- | INx logic "0" input bias current                 | $IN_x = \text{GND}$                                     | -                   | -                   | 1                   | $\mu\text{A}$ |
| $R_{pd}$                       | IN+, IN- | Inputs pull-down resistors                       | $IN_x = 5\text{ V}$                                     | 70                  | 100                 | 150                 | k $\Omega$    |
| <b>Driver buffer section</b>   |          |                                                  |                                                         |                     |                     |                     |               |
| $I_{GON}$                      | -        | Source short circuit current                     | $T_J = 25^\circ\text{C}$                                | -                   | 4                   | -                   | A             |
|                                |          |                                                  | $T_J = -40\text{ to }+125^\circ\text{C}$ <sup>(1)</sup> | 3                   | -                   | 5                   | A             |

| Symbol                             | Pin | Parameter                        | Test conditions                               | Min.    | Typ.     | Max. | Unit |
|------------------------------------|-----|----------------------------------|-----------------------------------------------|---------|----------|------|------|
| V <sub>GONH</sub>                  | -   | Source output high level voltage | I <sub>GON</sub> = 100 mA                     | VH-0.15 | VH-0.125 | -    | V    |
| R <sub>GON</sub>                   | -   | Source R <sub>DS_ON</sub>        | I <sub>GON</sub> = 100 mA                     | -       | 1.25     | 1.5  | Ω    |
| I <sub>GOFF</sub>                  | -   | Sink short-circuit current       | T <sub>J</sub> = 25°C                         | -       | 4        | -    | A    |
|                                    |     |                                  | T <sub>J</sub> = -40 to +125°C <sup>(1)</sup> | 3       | -        | 5.5  |      |
| V <sub>GOFFL</sub>                 | -   | Sink output low level voltage    | I <sub>GOFF</sub> = 100 mA                    | -       | 100      | 120  | mV   |
| R <sub>GOFF</sub>                  | -   | Sink R <sub>DS_ON</sub>          | I <sub>GOFF</sub> = 100 mA                    | -       | 1.0      | 1.2  | Ω    |
| <b>Miller Clamp</b>                |     |                                  |                                               |         |          |      |      |
| V <sub>CLAMPth</sub>               | -   | CLAMP voltage threshold          | V <sub>CLAMP</sub> vs. GNDISO                 | 1.3     | 2        | 2.6  | V    |
| I <sub>CLAMP</sub>                 | -   | CLAMP short-circuit current      | V <sub>CLAMP</sub> = 15V                      |         |          |      | A    |
|                                    |     |                                  | T <sub>J</sub> = 25°C                         | -       | 4        | -    |      |
|                                    |     |                                  | T <sub>J</sub> = -40 to +125°C <sup>(1)</sup> | 2       | -        | 5    |      |
| V <sub>CLAMP_L</sub>               | -   | CLAMP low level output voltage   | I <sub>CLAMP</sub> = 100mA                    | -       | 96       | 115  | mV   |
| R <sub>CLAMP</sub>                 | -   | CLAMP R <sub>DS_ON</sub>         | I <sub>CLAMP</sub> = 100mA                    | -       | 0.96     | 1.15 | Ω    |
| <b>Over-temperature protection</b> |     |                                  |                                               |         |          |      |      |
| T <sub>SD</sub>                    | -   | Shutdown temperature             | -                                             | 170     | -        | -    | °C   |
| T <sub>hys</sub>                   | -   | Temperature hysteresis           | -                                             | -       | 20       | -    | °C   |
| <b>Standby</b>                     |     |                                  |                                               |         |          |      |      |
| t <sub>STBY</sub>                  | -   | Standby time                     | See Section 6.3                               | 200     | 280      | 500  | μs   |
| t <sub>WUP</sub>                   | -   | Wake-up time                     | See Section 6.3                               | 10      | 20       | 35   | μs   |
| t <sub>awake</sub>                 | -   | Wake-up delay                    | See Section 6.3                               | 90      | 140      | 200  | μs   |
| t <sub>stbyfilt</sub>              | -   | Standby filter                   | See Section 6.3                               | 200     | 280      | 800  | ns   |

1. Characterization data, not tested in production.

## 5 Isolation

**Table 6. Isolation and safety specifications**

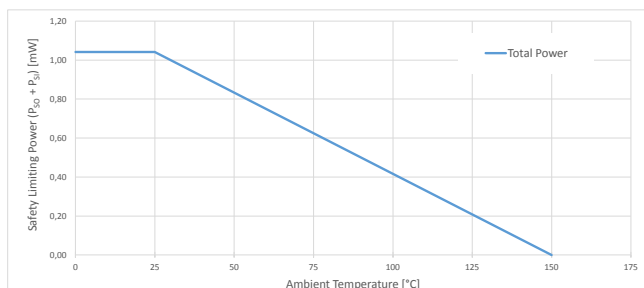
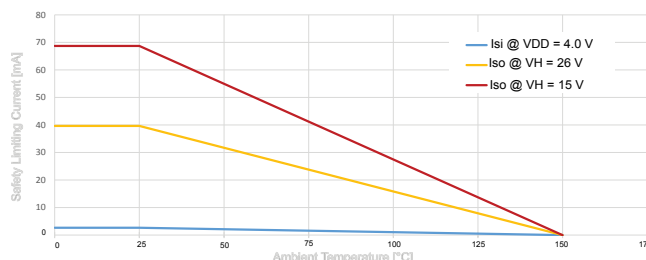
| Symbol                                                                      | Parameter                                           | Test Conditions                                                                                              | Value              | Unit              |
|-----------------------------------------------------------------------------|-----------------------------------------------------|--------------------------------------------------------------------------------------------------------------|--------------------|-------------------|
| General                                                                     |                                                     |                                                                                                              |                    |                   |
| CLR                                                                         | Clearance<br>(Minimum external air Gap)             | Measured from input terminals to output terminals, shortest distance trough air                              | 8                  | mm                |
| CPG                                                                         | Creepage<br>(Minimum External Tracking)             | Measured from input terminals to output terminals, shortest distance path along body                         | 8                  | mm                |
| CTI                                                                         | Comparative Tracking Index<br>(Tracking Resistance) | IEC 60112                                                                                                    | ≥ 400              | V                 |
| -                                                                           | Material Group                                      | According to IEC 60664-1                                                                                     | II                 | -                 |
| -                                                                           | Overvoltage Category per IEC 60664-1                | Rated mains voltages ≤ 150 V <sub>RMS</sub>                                                                  | I - IV             | -                 |
|                                                                             |                                                     | Rated mains voltages ≤ 300 V <sub>RMS</sub>                                                                  | I - III            | -                 |
|                                                                             |                                                     | Rated mains voltages ≤ 600 V <sub>RMS</sub>                                                                  | I - II             | -                 |
|                                                                             |                                                     | Rated mains voltages ≤ 1000 V <sub>RMS</sub>                                                                 | I                  | -                 |
| DIN EN IEC 60747-17 (VDE 0884-17)                                           |                                                     |                                                                                                              |                    |                   |
| V <sub>IORM</sub>                                                           | Maximum Repetitive Isolation Voltage                | AC voltage                                                                                                   | 1200               | V <sub>PEAK</sub> |
| V <sub>IOWM</sub>                                                           | Maximum Working Isolation Voltage                   | AC voltage (sinewave)                                                                                        | 850                | V <sub>RMS</sub>  |
|                                                                             |                                                     | DC voltage                                                                                                   | 1200               | V <sub>PEAK</sub> |
| V <sub>PR</sub>                                                             | Partial Discharge test voltage                      | Method a, Type and sample test<br>t <sub>m</sub> = 10 s<br>Partial discharge < 5 pC                          | 1920               | V <sub>PEAK</sub> |
|                                                                             |                                                     | Method b1, 100% Production test<br>t <sub>m</sub> = 1 s<br>Partial discharge < 5 pC                          | 2250               | V <sub>PEAK</sub> |
| V <sub>IOTM</sub>                                                           | Maximum Transient Isolation Voltage                 | Method a, Type and sample test<br>t <sub>ini</sub> = 60 s                                                    | 5000               | V <sub>PEAK</sub> |
| V <sub>IOTM,test</sub>                                                      | Transient Isolation Voltage test                    | Method b1, 100% Production test<br>V <sub>IOTM,test</sub> = V <sub>IOTM</sub> × 1.2, t <sub>ini</sub> = 1 s  | 6000               | V <sub>PEAK</sub> |
| V <sub>IMP</sub>                                                            | Maximum Impulse Voltage                             | Type test; Tested in air<br>1.2/50 μs waveform per IEC 62368-1                                               | 4600               | V <sub>PEAK</sub> |
| V <sub>IOSM</sub>                                                           | Maximum Surge isolation Voltage                     | Type test; Tested in oil<br>1.2/50 μs waveform per IEC 62368-1<br>V <sub>IOSM</sub> ≥ V <sub>IMP</sub> × 1.3 | 6000               | V <sub>PEAK</sub> |
| R <sub>IO</sub>                                                             | isolation Resistance                                | Type test; V <sub>IO</sub> = 500 V<br>T <sub>amb</sub> = 25 °C                                               | > 10 <sup>12</sup> | Ω                 |
|                                                                             |                                                     | Type and Sample test; V <sub>IO</sub> = 500 V<br>T <sub>amb,max</sub> = 125 °C                               | > 10 <sup>11</sup> |                   |
|                                                                             |                                                     | Type and Sample test; V <sub>IO</sub> = 500 V<br>T <sub>amb</sub> = T <sub>stg</sub> = 150 °C                | > 10 <sup>9</sup>  |                   |
| IEC 60747-17 certified for basic insulation. Certification number 40057398. |                                                     |                                                                                                              |                    |                   |

| Symbol                                                                           | Parameter                   | Test Conditions      | Value       | Unit                 |
|----------------------------------------------------------------------------------|-----------------------------|----------------------|-------------|----------------------|
| <b>UL-1577</b>                                                                   |                             |                      |             |                      |
| $V_{ISO}$                                                                        | Isolation Withstand voltage | 60 s; Type test      | 3540 / 5000 | $V_{RMS} / V_{PEAK}$ |
| $V_{ISO, test}$                                                                  | Isolation Voltage test      | 1 s; 100% production | 4240 / 6000 | $V_{RMS} / V_{PEAK}$ |
| Recognized under the UL 1577 Component Recognition Program - file number E362869 |                             |                      |             |                      |

**Table 7. Safety limits**

| Symbol   | Parameter                        | Test condition                                                                                                                                             | Min. | Typ. | Max. | Unit |
|----------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $T_S$    | Safety temperature               |                                                                                                                                                            |      |      | 150  | °C   |
| $P_{SI}$ | Maximum input power dissipation  | $R_{th(JA)} = 120 \text{ }^{\circ}\text{C/W}$<br>$T_{amb} = 25 \text{ }^{\circ}\text{C}, T_J = 150 \text{ }^{\circ}\text{C}$<br>$VDD = 5.5 \text{ V}$      |      |      | 15   | mW   |
| $P_{SO}$ | Maximum output power dissipation | $R_{th(JA)} = 120 \text{ }^{\circ}\text{C/W}$<br>$T_{amb} = 25 \text{ }^{\circ}\text{C}, T_J = 150 \text{ }^{\circ}\text{C}$                               |      |      | 1.03 | W    |
| $I_{SI}$ | Maximum input current            | $R_{th(JA)} = 120 \text{ }^{\circ}\text{C/W}$<br>$T_{amb} = 25 \text{ }^{\circ}\text{C}, T_J = 150 \text{ }^{\circ}\text{C}$<br>$VDD = 5.5 \text{ V}$      |      |      | 2.68 | mA   |
| $I_{SO}$ | Maximum output current           | $R_{th(JA)} = 120 \text{ }^{\circ}\text{C/W}$<br>$T_{amb} = 25 \text{ }^{\circ}\text{C}, T_J = 150 \text{ }^{\circ}\text{C}$<br>$VH-GNDISO = 26 \text{ V}$ |      |      | 39.9 | mA   |
|          |                                  | $R_{th(JA)} = 120 \text{ }^{\circ}\text{C/W}$<br>$T_{amb} = 25 \text{ }^{\circ}\text{C}, T_J = 150 \text{ }^{\circ}\text{C}$<br>$VH-GNDISO = 15 \text{ V}$ |      |      | 68.0 |      |

Safety limitations are aimed at minimizing potential damage to the isolation barrier upon failure of input or output circuitry. Without current limiting, excessive power dissipation might damage the die and the isolation barrier consequently. The maximum limits of  $P_S$  and  $I_S$  should not be exceeded. These limits vary with the ambient temperature  $T_{amb}$ , according to the related derating curves.

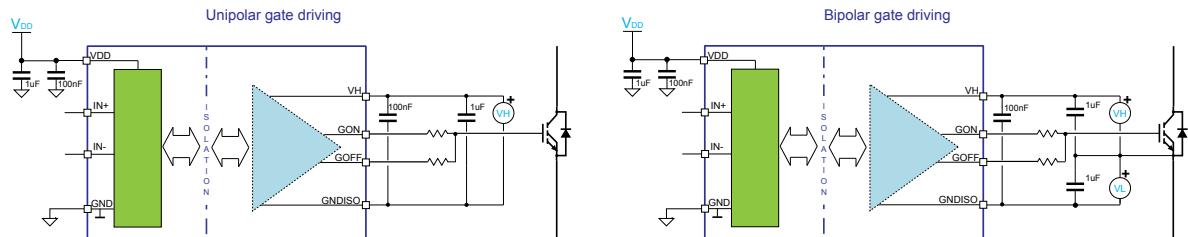
**Figure 5. Thermal derating curve for safety-related limiting power**

**Figure 6. Thermal derating curve for safety-related limiting current**


## 6 Functional description

### 6.1 Gate driving power supply and UVLO

The STGAP2HS is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

**Figure 7. Power supply configuration for unipolar and bipolar gate driving**



Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage falls below the VHoff threshold, the output buffer enters a “safe state”. When VH voltage reaches the VHon threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1  $\mu$ F and 10  $\mu$ F should be placed close to it.

### 6.2 Power-up, power-down and “safe state”

The following conditions define the “safe state”:

- GOFF = ON state;
- GON = High Impedance;
- CLAMP = ON state (for STGAP2HSC);

Such conditions are maintained at power-up of the isolated side ( $VH < VH_{on}$ ) and during whole device power down phase ( $VH < VH_{off}$ ), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage sides, the device output state depends on the status of the input pins.

### 6.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance with the truth table below.

**Table 8. Inputs truth table (applicable when device is not in UVLO or "safe state")**

| Input pins |     | Output pins |     |
|------------|-----|-------------|-----|
| IN+        | IN- | GON         | GOF |
| L          | L   | OFF         | ON  |
| H          | L   | ON          | OFF |
| L          | H   | OFF         | ON  |
| H          | H   | OFF         | ON  |

A deglitch filter prevents short noise spikes potentially present in the application from generating unwanted output commutations.

### 6.4 Miller Clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the  $C_{GD}$  capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin. The CLAMP switch is activated when gate voltage goes below the voltage threshold,  $V_{CLAMPth}$ , thus creating a low impedance path between the switch gate and the GNDISO pin.

### 6.5 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in "safe state" until communication link is properly established again.

### 6.6 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the  $T_{SD}$  temperature threshold, the device is forced in "safe state". The device operation is restored as soon as the junction temperature is lower than  $T_{SD}-T_{hys}$ .

## 6.7 Standby function

In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to  $I_{QDDSBY}$  and  $I_{QHDSBY}$  respectively, and the output remains in “safe state” (the output is actively forced low).

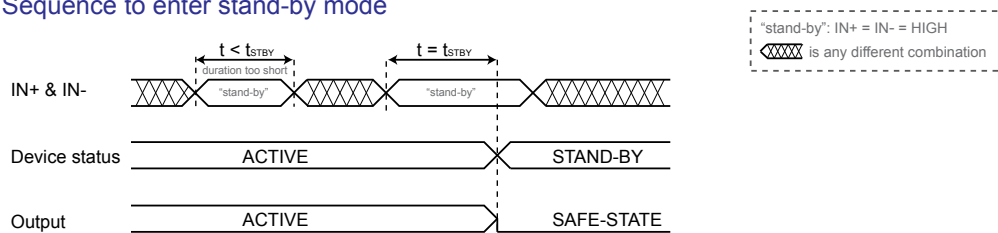
The way to enter standby is to keep both IN+ and IN- high (“standby” value) for a time longer than  $t_{STBY}$ . During stand-by the inputs can change from the “standby” value.

To exit stand-by, IN+ and IN- must be put in any combination different from the “standby” value for a time longer than  $t_{stbyfilt}$ , and then in the “standby” value for a time  $t$  such that  $t_{WUP} < t < t_{STBY}$ .

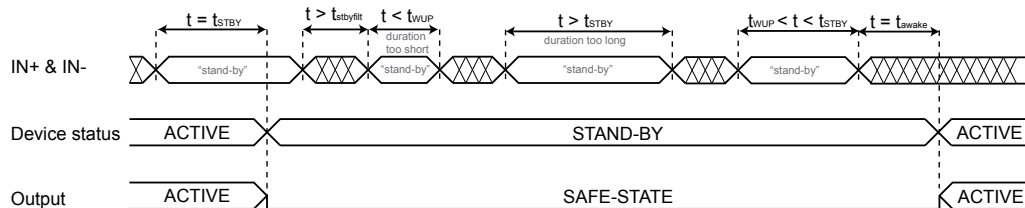
When the input configuration is changed from the “standby” value the output is enabled and set according to inputs state after a time  $t_{awake}$ .

**Figure 8. Standby state sequences**

### Sequence to enter stand-by mode

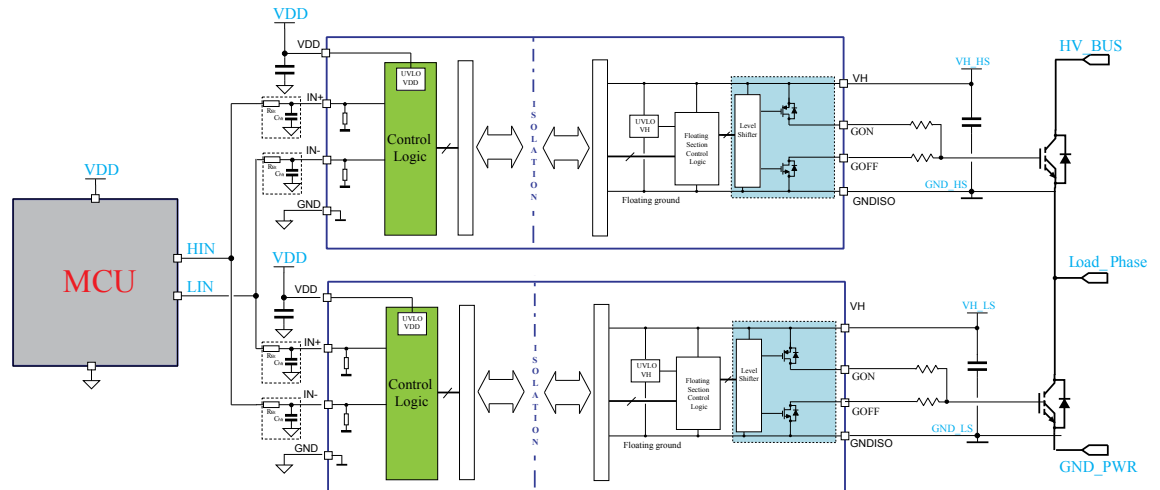


### Sequence to exit stand-by mode

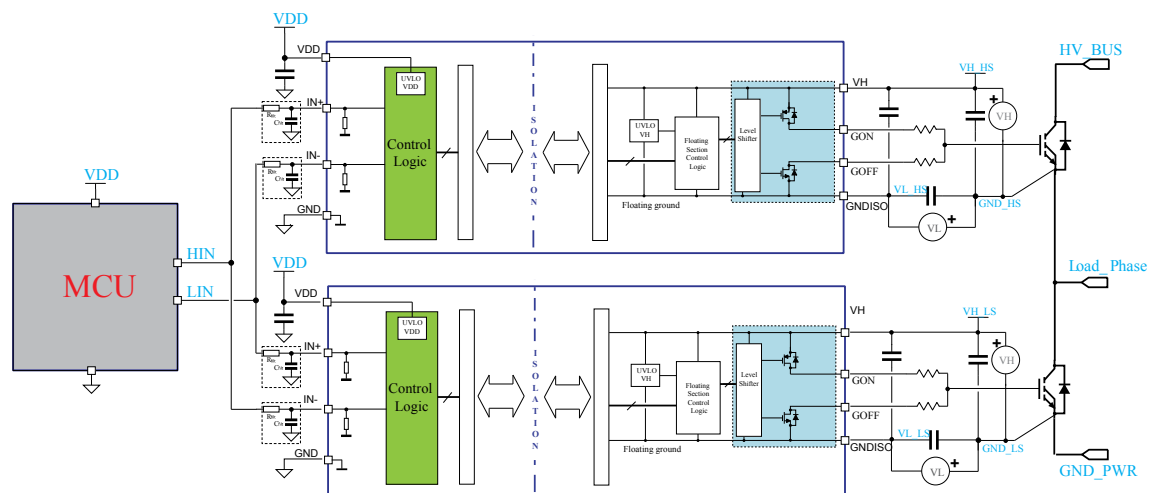


## 7 Typical application diagram

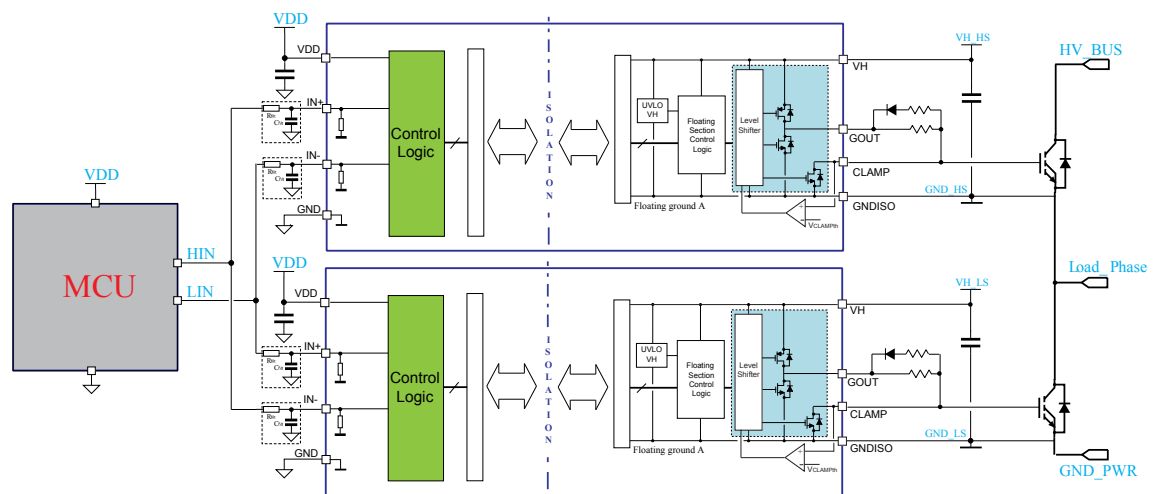
**Figure 9. Typical application diagram - Separated outputs**



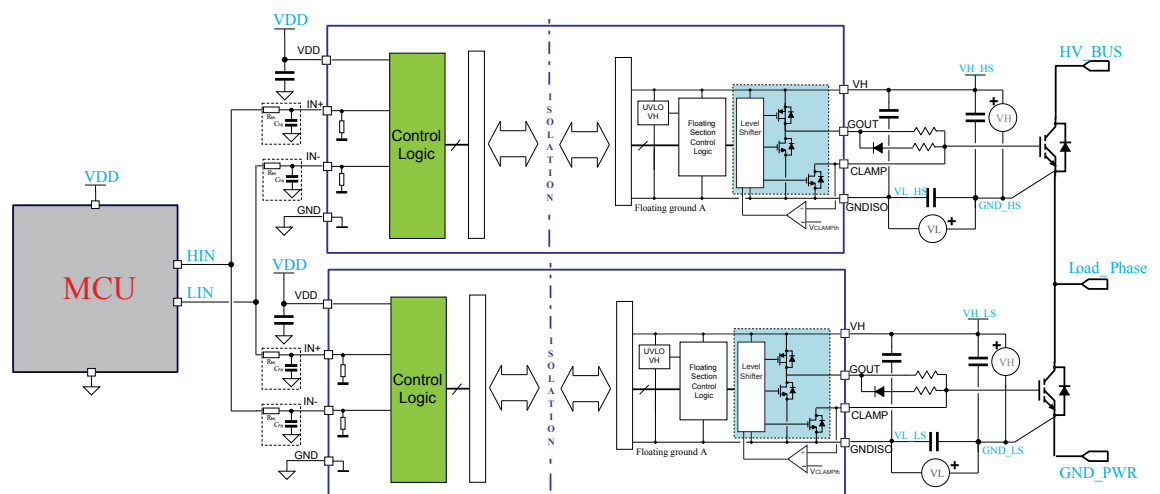
**Figure 10. Typical application diagram - Separated outputs and negative gate driving**



**Figure 11. Typical application diagram - Miller Clamp**



**Figure 12. Typical application diagram - Miller Clamp and negative gate driving**



## 8 Layout

### 8.1 Layout guidelines and considerations

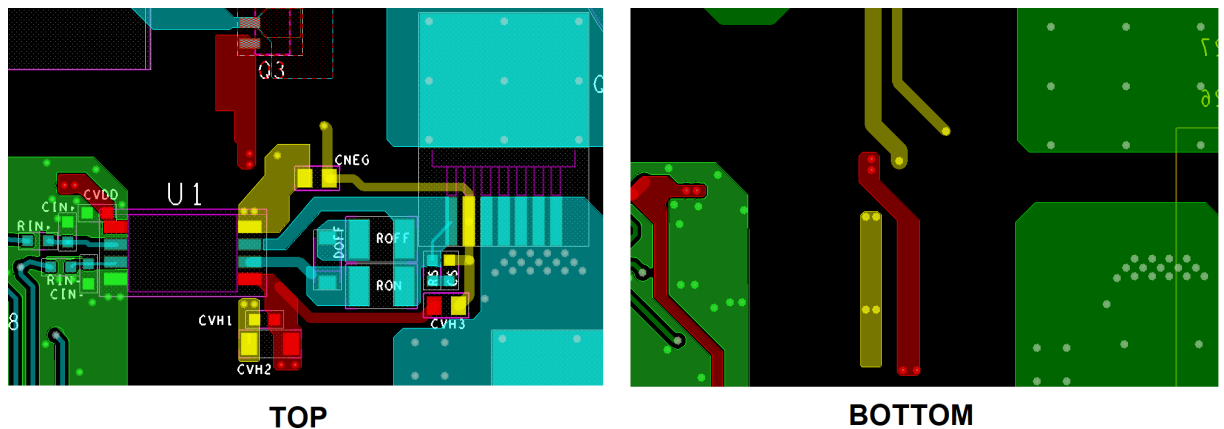
In order to optimize the PCB layout, the following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value between 1  $\mu$ F and 10  $\mu$ F should also be placed close to the supply pins.
- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver to minimize the gate loop area and inductance that might carry noise or cause ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

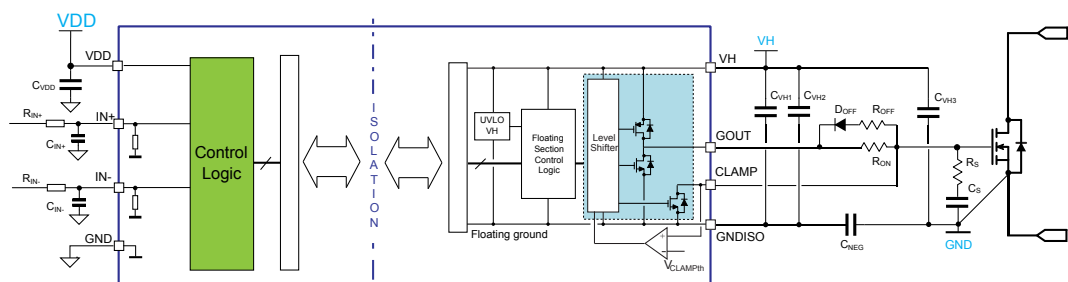
### 8.2 Layout example

An example of STGAP2HSC suggested PCB layout with main signals highlighted by different colors is shown in [Figure 13](#) (see [Figure 14](#) for reference schematic). It is recommended to follow this example for correct positioning and connection of filtering capacitors.

**Figure 13. STGAP2HSC suggested PCB layout: top and bottom**



**Figure 14. STGAP2HSC reference schematic for suggested PCB layout**



## 9 Testing and characterization information

Figure 15. CMTI test circuit

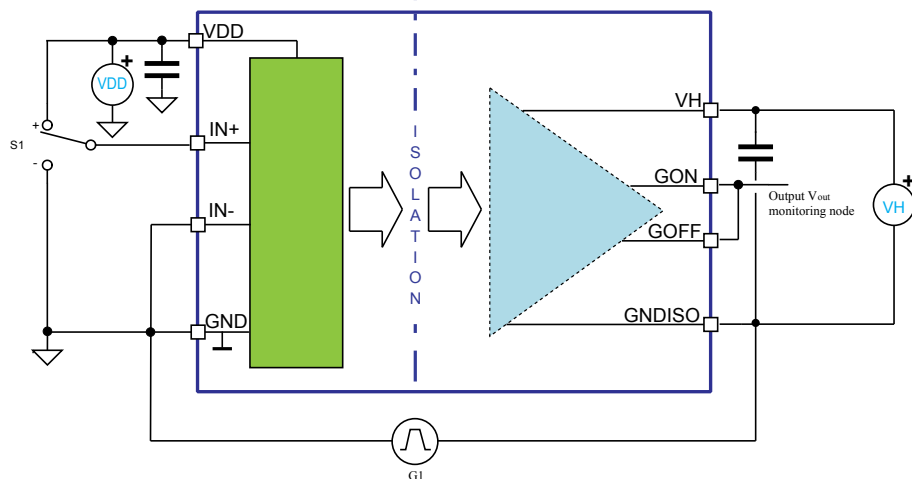
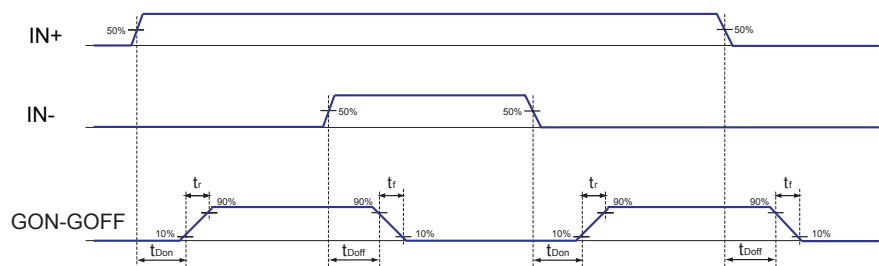


Figure 16. Timings definition



## 10 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

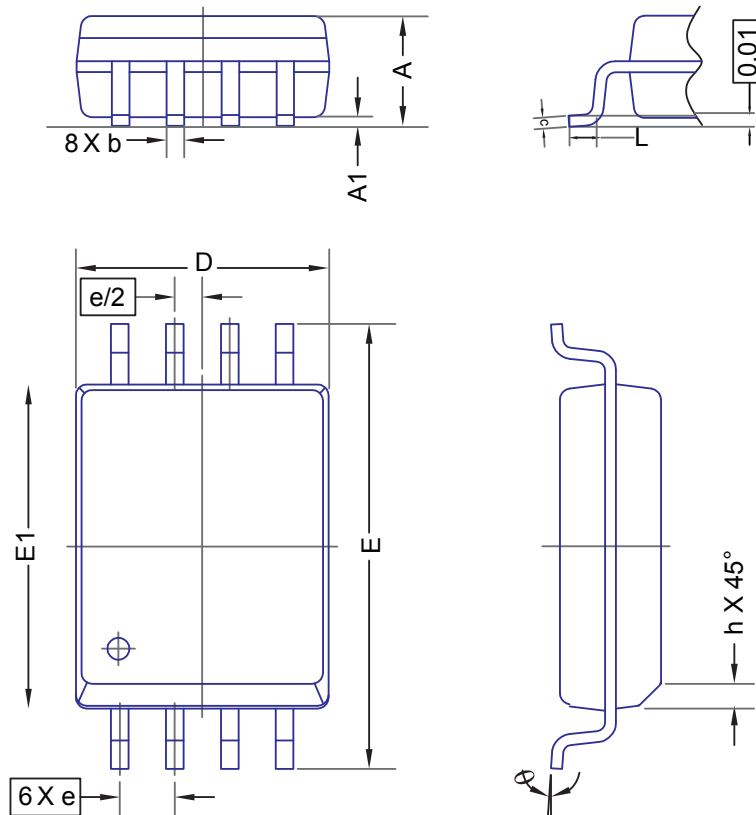
### 10.1 SO-8W package information

**Table 9. SO-8W package dimensions**

| Symbol           | Dimensions (mm) |      |       |
|------------------|-----------------|------|-------|
|                  | Min.            | Typ. | Max   |
| A                | 2.34            |      | 2.64  |
| A1               | 0.1             |      | 0.3   |
| b                | 0.3             |      | 0.51  |
| c                | 0.2             |      | 0.33  |
| D <sup>(1)</sup> | 5.64            |      | 6.05  |
| e                | 1.27 BSC        |      |       |
| E1               | 7.39            |      | 7.59  |
| E                | 10.11           |      | 10.52 |
| L                | 0.61            |      | 0.91  |
| h                | 0.25            |      | 0.76  |
| Θ                | 0°              |      | 8°    |
| aaa              | 0.25            |      |       |
| bbb              | 0.25            |      |       |
| ccc              | 0.1             |      |       |

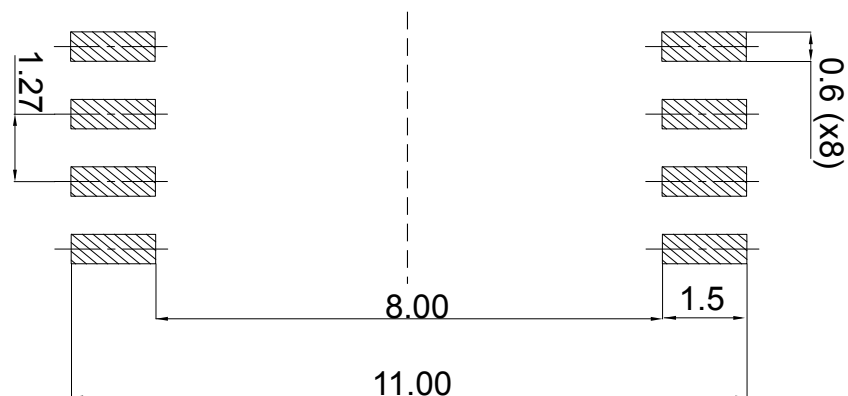
1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

**Figure 17. SO-8W mechanical data**



## 10.2 SO-8W suggested land pattern

**Figure 18. SO-8W suggested land pattern**



## 11 Ordering information

**Table 10. Device summary**

| Order code   | Output configuration | Package marking | Package | Packing       |
|--------------|----------------------|-----------------|---------|---------------|
| STGAP2HSMTR  | GON-GOFF             | GAP2HS2         | SO-8W   | Tape and Reel |
| STGAP2HSCMTR | GOUT-CLAMP           | GAP2HSC2        | SO-8W   | Tape and Reel |

## Revision history

**Table 11. Document revision history**

| Date        | Version | Changes                                                                                                                                                                                                                                                                                                                                                                        |
|-------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-Aug-2020 | 1       | Initial release.                                                                                                                                                                                                                                                                                                                                                               |
| 01-Sep-2020 | 2       | Updated some parameters in <a href="#">Table 5</a> ; updated some symbols in <a href="#">Table 9</a>                                                                                                                                                                                                                                                                           |
| 13-Aug-2021 | 3       | Updated VDD parameter in <a href="#">Table 3</a> ; updated Isolation Resistance Test condition parameter and title of UL1577 section in <a href="#">Section 5</a> ; changed <a href="#">Figure 18</a> and <a href="#">Figure 12</a> ; updated <a href="#">Table 4</a> ; updated <a href="#">Driver buffer section</a> and <a href="#">Standby</a> in <a href="#">Table 5</a> . |
| 15-Oct-2021 | 4       | Updated <a href="#">Table 5</a> with missing notes.                                                                                                                                                                                                                                                                                                                            |
| 29-Sep-2022 | 5       | Added UL file certification.                                                                                                                                                                                                                                                                                                                                                   |
| 27-Jan-2026 | 6       | Added IEC 60747-17 certification: updated <a href="#">Section Features</a> and <a href="#">Section 5</a> ; updated <a href="#">Cover image</a> , <a href="#">Section 6.3</a> and <a href="#">Section 8.2</a> .<br>Updated <a href="#">Table 2</a> ( $T_{stg}$ symbol), <a href="#">Table 3</a> (added $T_{amb}$ ).                                                             |

## Contents

|           |                                                 |           |
|-----------|-------------------------------------------------|-----------|
| <b>1</b>  | <b>Block diagram</b>                            | <b>3</b>  |
| <b>2</b>  | <b>Pin description and connection diagram</b>   | <b>4</b>  |
| <b>3</b>  | <b>Electrical data</b>                          | <b>5</b>  |
| 3.1       | Absolute maximum ratings                        | 5         |
| 3.2       | Recommended operating conditions                | 5         |
| 3.3       | Thermal data                                    | 5         |
| <b>4</b>  | <b>Electrical characteristics</b>               | <b>6</b>  |
| <b>5</b>  | <b>Isolation</b>                                | <b>8</b>  |
| <b>6</b>  | <b>Functional description</b>                   | <b>10</b> |
| 6.1       | Gate driving power supply and UVLO              | 10        |
| 6.2       | Power-up, power-down and “safe state”           | 10        |
| 6.3       | Control inputs                                  | 11        |
| 6.4       | Miller Clamp function                           | 11        |
| 6.5       | Watchdog                                        | 11        |
| 6.6       | Thermal shutdown protection                     | 11        |
| 6.7       | Standby function                                | 12        |
| <b>7</b>  | <b>Typical application diagram</b>              | <b>13</b> |
| <b>8</b>  | <b>Layout</b>                                   | <b>15</b> |
| 8.1       | Layout guidelines and considerations            | 15        |
| 8.2       | Layout example                                  | 15        |
| <b>9</b>  | <b>Testing and characterization information</b> | <b>16</b> |
| <b>10</b> | <b>Package information</b>                      | <b>17</b> |
| 10.1      | SO-8W package information                       | 17        |
| 10.2      | SO-8W suggested land pattern                    | 18        |
| <b>11</b> | <b>Ordering information</b>                     | <b>19</b> |
|           | <b>Revision history</b>                         | <b>20</b> |
|           | <b>List of tables</b>                           | <b>22</b> |
|           | <b>List of figures</b>                          | <b>23</b> |

## List of tables

|                  |                                                                                      |    |
|------------------|--------------------------------------------------------------------------------------|----|
| <b>Table 1.</b>  | Pin Description . . . . .                                                            | 4  |
| <b>Table 2.</b>  | Absolute maximum ratings . . . . .                                                   | 5  |
| <b>Table 3.</b>  | Recommended operating conditions. . . . .                                            | 5  |
| <b>Table 4.</b>  | Thermal data. . . . .                                                                | 5  |
| <b>Table 5.</b>  | Electrical characteristics . . . . .                                                 | 6  |
| <b>Table 6.</b>  | Isolation and safety specifications . . . . .                                        | 8  |
| <b>Table 7.</b>  | Safety limits . . . . .                                                              | 9  |
| <b>Table 8.</b>  | Inputs truth table (applicable when device is not in UVLO or "safe state") . . . . . | 11 |
| <b>Table 9.</b>  | SO-8W package dimensions . . . . .                                                   | 17 |
| <b>Table 10.</b> | Device summary . . . . .                                                             | 19 |
| <b>Table 11.</b> | Document revision history . . . . .                                                  | 20 |

## List of figures

|                   |                                                                                     |    |
|-------------------|-------------------------------------------------------------------------------------|----|
| <b>Figure 1.</b>  | Block diagram - Single output and Miller Clamp configuration . . . . .              | 3  |
| <b>Figure 2.</b>  | Block diagram - Separate output configuration . . . . .                             | 3  |
| <b>Figure 3.</b>  | Pin connection (top view) - Single output and Miller CLAMP option . . . . .         | 4  |
| <b>Figure 4.</b>  | Pin connection (top view) - Separated outputs option. . . . .                       | 4  |
| <b>Figure 5.</b>  | Thermal derating curve for safety-related limiting power. . . . .                   | 9  |
| <b>Figure 6.</b>  | Thermal derating curve for safety-related limiting current . . . . .                | 9  |
| <b>Figure 7.</b>  | Power supply configuration for unipolar and bipolar gate driving . . . . .          | 10 |
| <b>Figure 8.</b>  | Standby state sequences. . . . .                                                    | 12 |
| <b>Figure 9.</b>  | Typical application diagram - Separated outputs . . . . .                           | 13 |
| <b>Figure 10.</b> | Typical application diagram - Separated outputs and negative gate driving . . . . . | 13 |
| <b>Figure 11.</b> | Typical application diagram - Miller Clamp . . . . .                                | 14 |
| <b>Figure 12.</b> | Typical application diagram - Miller Clamp and negative gate driving . . . . .      | 14 |
| <b>Figure 13.</b> | STGAP2HSC suggested PCB layout: top and bottom . . . . .                            | 15 |
| <b>Figure 14.</b> | STGAP2HSC reference schematic for suggested PCB layout . . . . .                    | 15 |
| <b>Figure 15.</b> | CMTI test circuit . . . . .                                                         | 16 |
| <b>Figure 16.</b> | Timings definition . . . . .                                                        | 16 |
| <b>Figure 17.</b> | SO-8W mechanical data . . . . .                                                     | 18 |
| <b>Figure 18.</b> | SO-8W suggested land pattern. . . . .                                               | 18 |

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