Galvanically isolated 4 A single gate driver for SiC MOSFETs

SO-8W

Product status link
STGAP2SICS

Product label
SUSTAINABLE TECHNOLOGY

Features

- Driver current capability: 4 A sink/source @25°C
- 100 V/ns Common Mode Transient Immunity (CMTI)
- Overall input-output propagation delay: 75 ns
- Separate sink and source option for easy gate driving configuration
- 4 A Miller CLAMP dedicated pin option
- UVLO function
- Gate driving voltage up to 26 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shut-down protection
- Standby function
- Wide body SO-8W package
- Galvanic isolation IEC 60747-17 certified, UL 1577 recognized
  - Maximum Repetitive Isolation Voltage V_{IORM} = 1.2 kV_{PEAK}
  - Transient Overvoltage V_{IOTM} = 5.0 kV_{PEAK}
  - Isolation voltage V_{ISO} = 3.5 kV_{RMS}

Applications

- Motor driver for home appliances, factory automation, industrial drives and fans.
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units
- DC-DC converters
- Power Factor Correction

Description

The STGAP2SICS is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for mid and high power applications such as power conversion and motor driver inverters in industrial applications. The device is available in two different configurations. The configuration with separated output pins allows to independently optimize turn-on and turn-off by using dedicated gate resistors. The configuration featuring single output pin and Miller CLAMP function prevents gate spikes during fast commutations in half-bridge topologies. Both configurations provide high flexibility and bill of material reduction for external components.

The device integrates protection functions: UVLO with optimized value for SiC MOSFETs and thermal shut down are included to facilitate the design of highly reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction. The input to output propagation delay is less than 75 ns, which delivers high PWM control accuracy. A standby mode is available to reduce idle power consumption.

1 Block diagram

Figure 1. Block diagram - Single output and Miller Clamp configuration

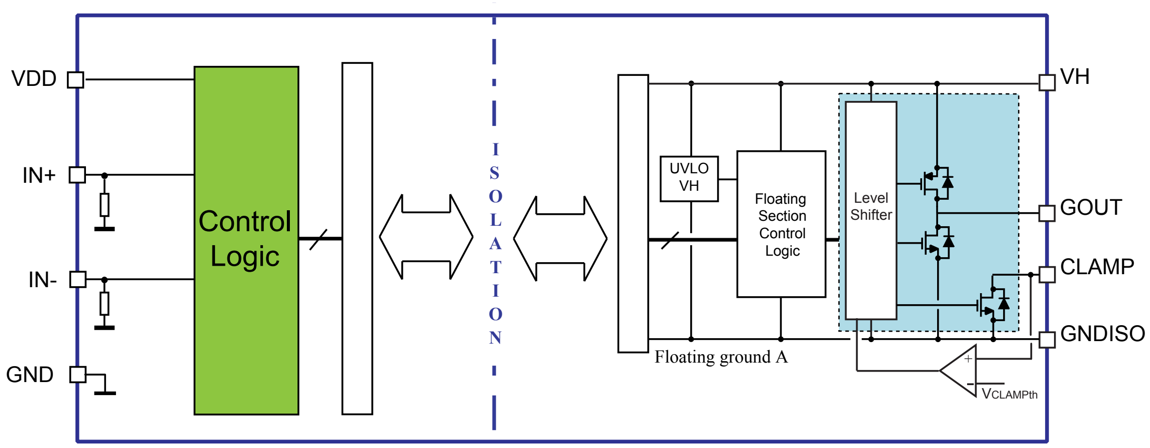
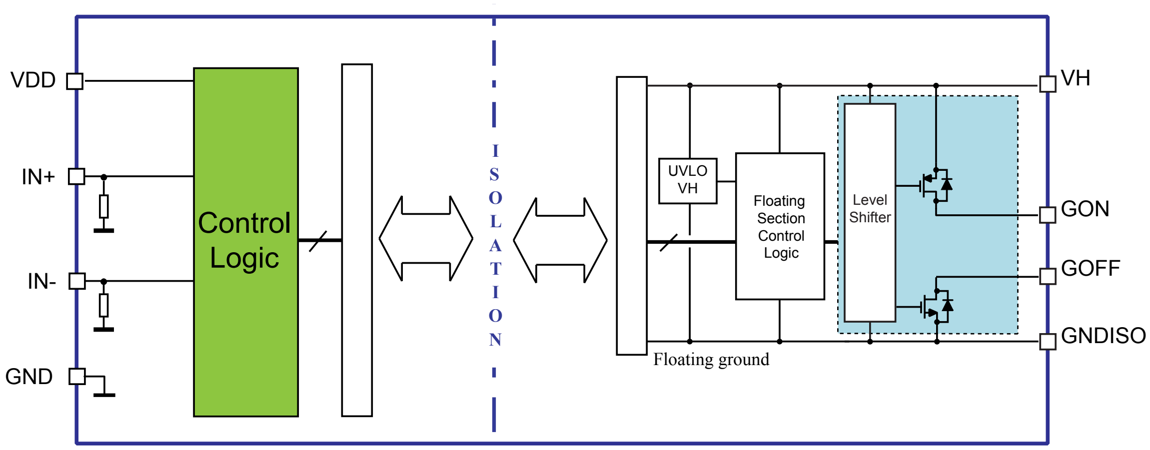


Figure 2. Block diagram - Separate output configuration



2 Pin description and connection diagram

Figure 3. Pin connection (top view) - Single output and Miller CLAMP option

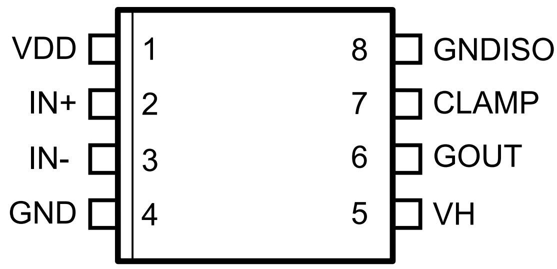


Figure 4. Pin connection (top view) - Separated outputs option

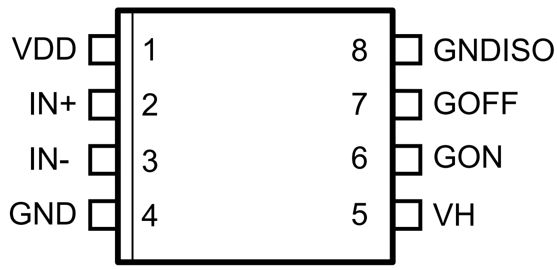


Table 1. Pin Description

Pin #		Pin Name	Type	Function
Figure 4	Figure 3			
1	1	VDD	Power Supply	Driver logic supply voltage.
2	2	IN+	Logic Input	Driver logic input, active high.
3	3	IN-	Logic Input	Driver logic input, active low.
4	4	GND	Power Supply	Driver logic ground.
5	5	VH	Power Supply	Gate driving positive voltage supply.
-	6	GOUT	Analog Output	Sink/Source output.
-	7	CLAMP	Analog Output	Active Miller Clamp.
6	-	GON	Analog Output	Source output.
7	-	GOFF	Analog Output	Sink output.
8	8	GNDISO	Power Supply	Gate driving Isolated ground.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	-0.3	6.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	-0.3	6.5	V
VH	Positive supply voltage (VH vs. GNDISO)	-	-0.3	28	V
V_{OUT}	Voltage on gate driver outputs (GON, GOFF, CLAMP VS. GNDISO)	-	-0.3	VH+0.3	V
T_J	Junction temperature	-	-40	150	°C
T_{stg}	Storage temperature	-	-50	150	°C
ESD	HBM (human body model)	-	2		kV

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-	3.1	5.5	V
V_{LOGIC}	Logic pins voltage vs. GND	-	0	5.5	V
VH	Positive supply voltage (VH vs. GNDISO)	-	Max(VH_{ON})	26	V
F_{SW}	Maximum switching frequency(1)	-	-	1	MHz
t_{OUT}	Output pulse width (GOUT, GON-GOFF)	-	100	-	ns
T_J	Operating junction temperature	-	-40	125	°C
T_{amb}	Ambient temperature	-	-40	125	°C

1. *Actual limit depends on power dissipation and T_J.*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-8W	120	°C/W

4 Electrical characteristics

Testing conditions: T_J = 25°C, VH = 18 V, VDD = 5 V unless otherwise specified).

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	IN+, IN-	Input to output propagation delay ON	-	50	75	90	ns
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	-	50	75	90	ns
t_r	-	Rise time	CL = 4.7 nF See Figure 15	-	30	-	ns
t_f	-	Fall time		-	30	-	ns
PWD	-	Pulse Width Distortion $\lvert t_{Don}-t_{Doff}\rvert$	-	-	-	20	ns
$t_{deglitch}$	IN+, IN-	Inputs deglitch filter	-	-	20	40	ns
CMTI [(1)]	-	Common-mode transient immunity, $\lvert dV_{ISO}/dt\rvert$	V_{CM} = 1500 V, See Figure 16	100	-	-	V/ns
Supply voltage							
VH_{on}	-	VH UVLO turn-on threshold	-	14.6	15.5	16.4	V
VH_{off}	-	VH UVLO turn-off threshold	-	13.9	14.8	15.7	V
VH_{hyst}	-	VH UVLO hysteresis	-	600	750	950	mV
I_{QHU}	-	VH undervoltage quiescent supply current	VH = 7 V	-	1.3	1.8	mA
I_{QH}	-	VH quiescent supply current	-	-	1.3	1.8	mA
I_{QHSBY}	-	Standby VH quiescent supply current	Standby mode	-	400	550	µA
SafeClp	-	GOFF active clamp	I_{GOFF} = 0.2 A; VH floating	-	2	2.3	V
I_{QDD}	-	VDD quiescent supply current	-	-	1.0	1.3	mA
I_{QDDSBY}	-	Standby VDD quiescent supply current	Standby mode	-	40	65	µA
Logic Inputs							
V_{il}	IN+, IN-	Low level logic threshold voltage	-	0.29·VDD	0.33·VDD	0.37·VDD	V
V_{ih}	IN+, IN-	High level logic threshold voltage	-	0.62·VDD	0.66·VDD	0.70·VDD	V
I_{INh}	IN+, IN-	INx logic “1” input bias current	IN_x = 5 V	33	50	70	µA
I_{INl}	IN+, IN-	INx logic “0” input bias current	IN_x = GND	-	-	1	µA
R_{pd}	IN+, IN-	Inputs pull-down resistors	IN_x = 5 V	70	100	150	kΩ
Driver buffer section							
I_{GON}	-	Source short circuit current	T_J = 25°C	-	4	-	A
			T_J = -40 to +125°C [(1)]	3	-	5	A

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{GONH}	-	Source output high level voltage	I_{GON} = 100 mA	VH-0.15	VH-0.125	-	V
R_{GON}	-	Source R_{DS_ON}	I_{GON} = 100 mA	-	1.25	1.5	Ω
I_{GOFF}	-	Sink short-circuit current	T_J = 25°C	-	4	-	A
			T_J = -40 to +125°C (1)	3	-	5.5	
V_{GOFFL}	-	Sink output low level voltage	I_{GOFF} = 100 mA	-	100	120	mV
R_{GOFF}	-	Sink R_{DS_ON}	I_{GOFF} = 100 mA	-	1.0	1.2	Ω
Miller Clamp							
$V_{CLAMPth}$	-	CLAMP voltage threshold	V_{CLAMP} vs.GNDISO	1.3	2	2.6	V
I_{CLAMP}	-	CLAMP short-circuit current	V_{CLAMP} = 15V				A
			T_J = 25°C	-	4	-	
			T_J = -40 to +125°C (1)	2	-	5	
V_{CLAMP_L}	-	CLAMP low level output voltage	I_{CLAMP} = 100mA	-	96	115	mV
R_{CLAMP}	-	CLAMP R_{DS_ON}	I_{CLAMP} = 100mA	-	0.96	1.15	Ω
Over-temperature protection							
T_{SD}	-	Shutdown temperature	-	170	-	-	°C
T_{hys}	-	Temperature hysteresis	-	-	20	-	°C
Standby							
t_{STBY}	-	Standby time	See Section 6.3	200	280	500	µs
t_{WUP}	-	Wake-up time	See Section 6.3	10	20	35	µs
t_{awake}	-	Wake-up delay	See Section 6.3	90	140	200	µs
$t_{stbyfilt}$	-	Standby filter	See Section 6.3	200	280	800	ns

1. *Characterization data, not tested in production.*

5 Isolation

Table 6. Isolation and safety specifications

Symbol	Parameter	Test Conditions	Value	Unit
General				
CLR	Clearance (Minimum external air Gap)	Measured from input terminals to output terminals, shortest distance trough air	8	mm
CPG	Creepage (Minimum External Tracking)	Measured from input terminals to output terminals, shortest distance path along body	8	mm
CTI	Comparative Tracking Index (Tracking Resistance)	IEC 60112	≥ 400	V
-	Material Group	According to IEC 60664-1	II	-
-	Overvoltage Category per IEC 60664-1	Rated mains voltages ≤ 150 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 300 V_{RMS}	I - III	-
		Rated mains voltages ≤ 600 V_{RMS}	I - II	-
		Rated mains voltages ≤ 1000 V_{RMS}	I	-
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage	1200	V_{PEAK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage (sinewave)	850	V_{RMS}
		DC voltage	1200	V_{PEAK}
V_{PR}	Partial Discharge test voltage	Method a, Type and sample test t_m= 10 s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b1, 100% Production test t_m = 1 s Partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Maximum Transient Isolation Voltage	Method a, Type and sample test t_{ini} = 60 s	5000	V_{PEAK}
$V_{IOTM,test}$	Transient Isolation Voltage test	Method b1, 100% Production test $V_{IOTM,test} = V_{IOTM} \times 1.2$, t_{ini} = 1 s	6000	V_{PEAK}
V_{IMP}	Maximum Impulse Voltage	Type test; Tested in air 1.2/50 µs waveform per IEC 62368-1	4600	V_{PEAK}
V_{IOSM}	Maximum Surge isolation Voltage	Type test; Tested in oil 1.2/50 µs waveform per IEC 62368-1 $V_{IOSM} \geq V_{IMP} \times 1.3$	6000	V_{PEAK}
R_{IO}	isolation Resistance	Type test; V_{IO} = 500 V T_{amb} = 25 °C	> 10^{12}	Ω
		Type and Sample test; V_{IO} = 500 V $T_{amb,max}$ = 125 °C	> 10^{11}	
		Type and Sample test; V_{IO} = 500 V $T_{amb} = T_{stg}$ = 150 °C	> 10^{9}	
IEC 60747-17 certified for basic insulation. Certification number 40057398.				

Symbol	Parameter	Test Conditions	Value	Unit
UL-1577				
V_{ISO}	Isolation Withstand voltage	60 s; Type test	3540 / 5000	V_{RMS} / V_{PEAK}
$V_{ISO,test}$	Isolation Voltage test	1 s; 100% production	4240 / 6000	V_{RMS} / V_{PEAK}
Recognized under the UL 1577 Component Recognition Program - file number E362869				

Table 7. Safety limits

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_S	Safety temperature				150	°C
P_{SI}	Maximum input power dissipation	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150°C VDD = 5.5 V			14.75	mW
P_{SO}	Maximum output power dissipation	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150°C			1.03	W
I_{SI}	Maximum input current	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150°C VDD = 5.5 V			2.68	mA
I_{SO}	Maximum output current	$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150°C VH-GNDISO = 26 V			39.5	mA
		$R_{th(JA)}$ = 120 °C/W T_{amb} = 25 °C, T_J = 150 °C VH-GNDISO = 18 V			57.0	

Safety limitings are aimed at minimizing potential damage to the isolation barrier upon failure of input or output circuitry. Without current limiting, excessive power dissipation might damage the die and the isolation barrier consequently. The maximum limits of P_S and I_S should not be exceeded. These limits vary with the ambient temperature T_{amb}, according to the related derating curves.

Figure 5. Thermal derating curve for safety-related limiting power

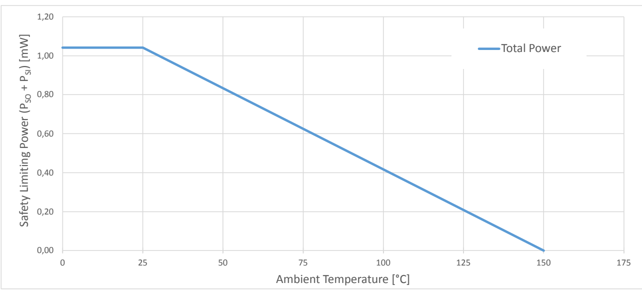
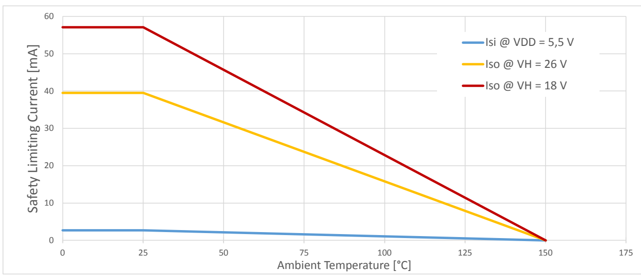


Figure 6. Thermal derating curve for safety-related limiting current

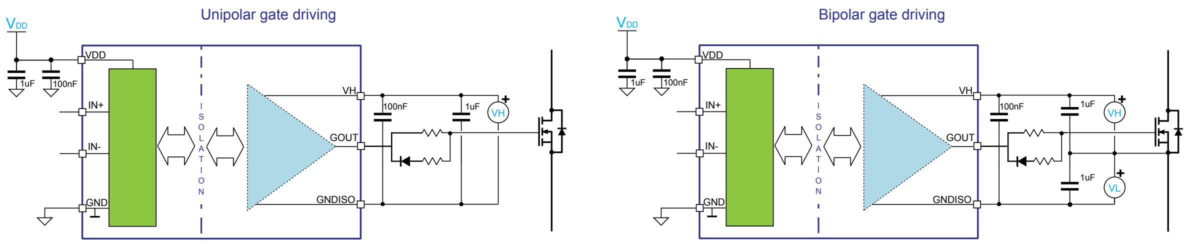


6 Functional description

6.1 Gate driving power supply and UVLO

The STGAP2SICS is a flexible and compact gate driver with 4 A output current and rail-to-rail outputs. The device allows implementation of either unipolar or bipolar gate driving.

Figure 7. Power supply configuration for unipolar and bipolar gate driving



Undervoltage protection is available on VH supply pin. A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

When VH voltage falls below the VHoff threshold, the output buffer enters a “safe state”. When VH voltage reaches the VHon threshold, the device returns to normal operation and sets the output according to actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering. The best filtering is obtained by using low-ESR SMT ceramic capacitors and are therefore recommended. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with value in the range between 1 μF and 10 μF should be placed close to it.

6.2 Power-up, power-down and “safe state”

The following conditions define the “safe state”:

- GOFF = ON state;
- GON = High Impedance;
- CLAMP = ON state (for STGAP2SICSC);

Such conditions are maintained at power-up of the isolated side ($VH < VH_{on}$) and during whole device power down phase ($VH < VH_{off}$), regardless of the value of the input pins.

The device integrates a structure which clamps the driver output to a voltage not higher than SafeClp when VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If VH positive supply pin is floating or not supplied the GOFF pin is therefore clamped to a voltage smaller than SafeClp.

If the supply voltage VDD of the control section of the device is not supplied, the output is put in safe state, and remains in such condition until the VDD voltage returns within operative conditions.

After power-up of both isolated and low voltage sides, the device output state depends on the status of the input pins.

6.3 Control inputs

The device is controlled through the IN+ and IN- logic inputs, in accordance with the truth table below.

Table 8. Inputs truth table (applicable when device is not in UVLO or "safe state")

Input pins		Output pins	
IN+	IN-	GON	GOFF
L	L	OFF	ON
H	L	ON	OFF
L	H	OFF	ON
H	H	OFF	ON

A deglitch filter prevents short noise spikes potentially present in the application from generating unwanted output commutations.

6.4 Miller Clamp function

The Miller clamp function allows the control of the Miller current during the power stage switching in half-bridge configurations. When the external power transistor is in the OFF state, the driver operates to avoid the induced turn-on phenomenon that may occur when the other switch in the same leg is being turned on, due to the C_{GD} capacitance.

During the turn-off period the gate of the external switch is monitored through the CLAMP pin. The CLAMP switch is activated when gate voltage goes below the voltage threshold, $V_{CLAMPth}$, thus creating a low impedance path between the switch gate and the GNDISO pin.

6.5 Watchdog

The isolated HV side has a watchdog function in order to identify when it is not able to communicate with LV side, for example because the VDD of the LV side is not supplied. In this case the output of the driver is forced in “safe state” until communication link is properly established again.

6.6 Thermal shutdown protection

The device provides a thermal shutdown protection. When junction temperature reaches the T_{SD} temperature threshold, the device is forced in “safe state”. The device operation is restored as soon as the junction temperature is lower than T_{SD}-T_{hys}.

6.7 Standby function

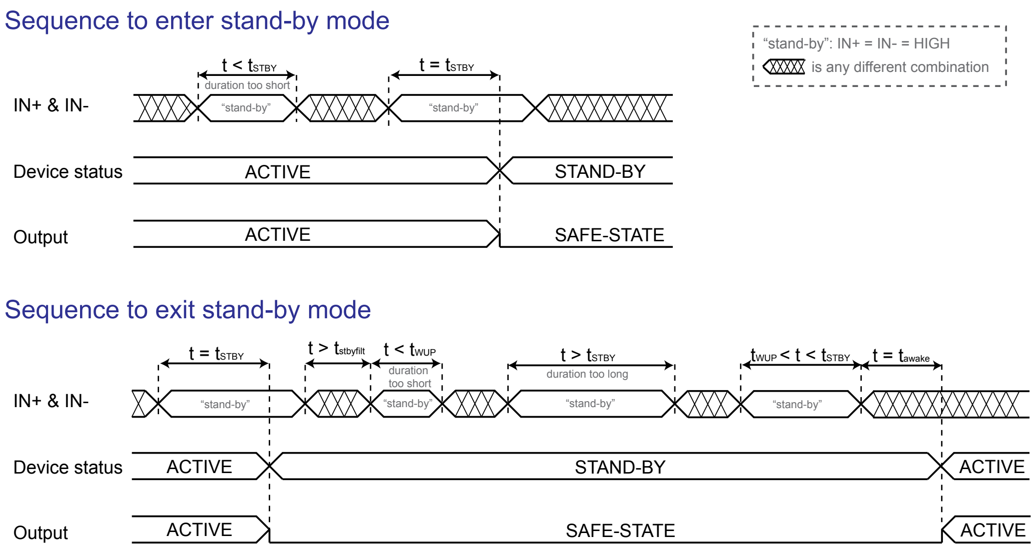
In order to reduce the power consumption of both control interface and gate driving sides the device can be put in standby mode. In standby mode the quiescent current from VDD and VH supply pins is reduced to I_{QDDSBY} and I_{QHSBY} respectively, and the output remains in "safe state" (the output is actively forced low).

The way to enter standby is to keep both IN+ and IN- high ("standby" value) for a time longer than t_{STBY}. During stand-by the inputs can change from the "standby" value.

To exit stand-by, IN+ and IN- must be put in any combination different from the "standby" value for a time longer than $t_{stbyfilt}$, and then in the "standby" value for a time t such that t_{WUP}<t <t_{STBY}.

When the input configuration is changed from the "standby" value the output is enabled and set according to inputs state after a time t_{awake}.

Figure 8. Standby state sequences



7 Typical application diagram

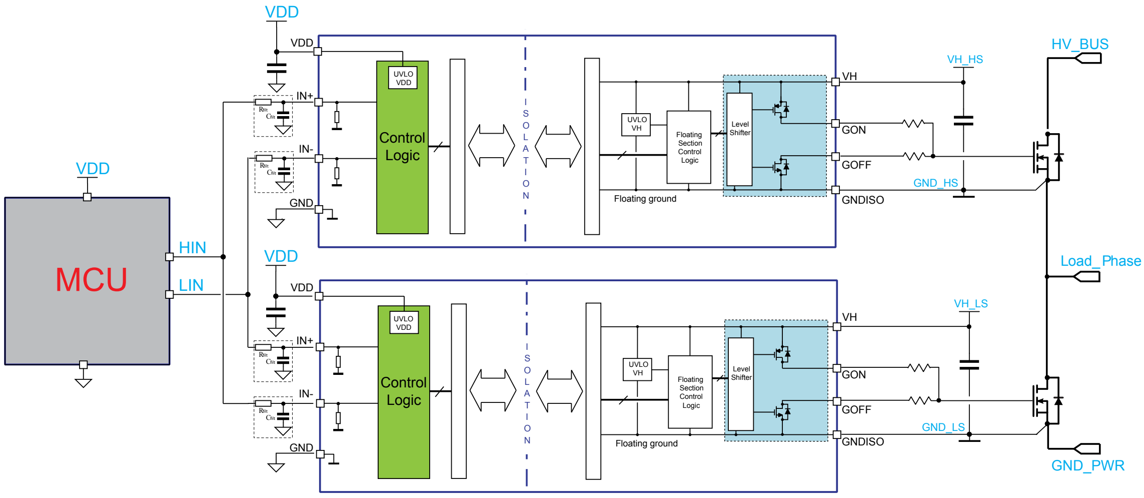


Figure 9. Typical application diagram - Separated outputs

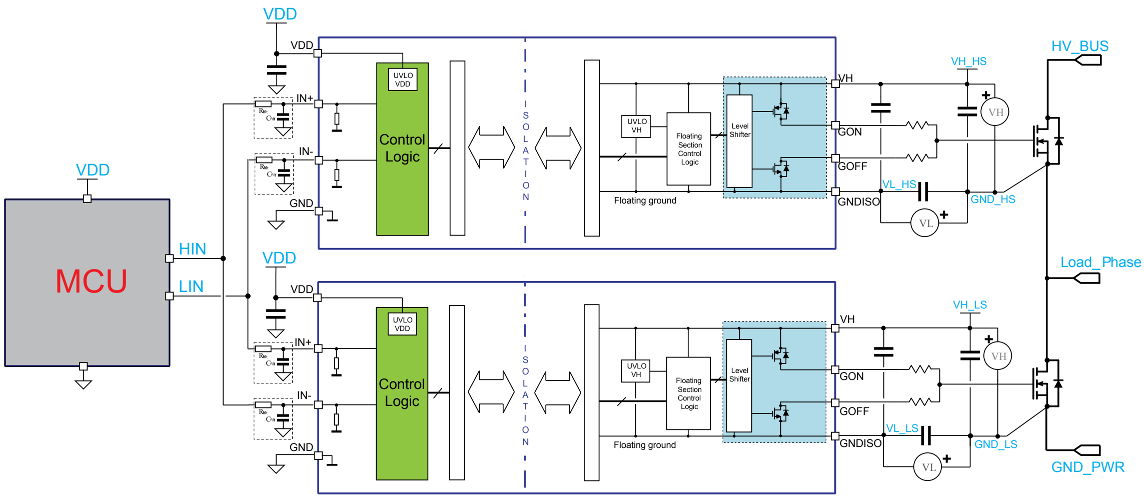


Figure 10. Typical application diagram - Separated outputs and negative gate driving

Figure 11. **Typical application diagram - Miller Clamp**

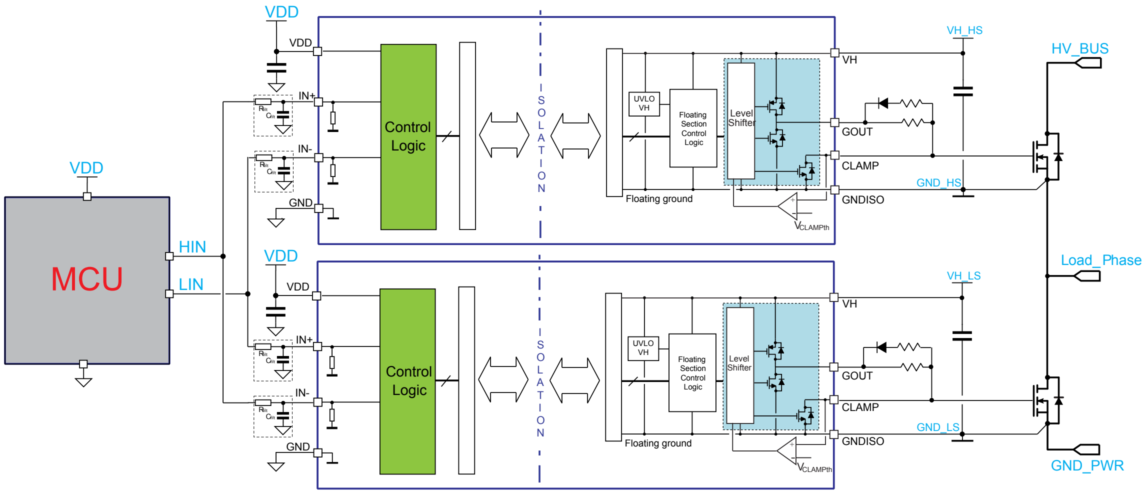
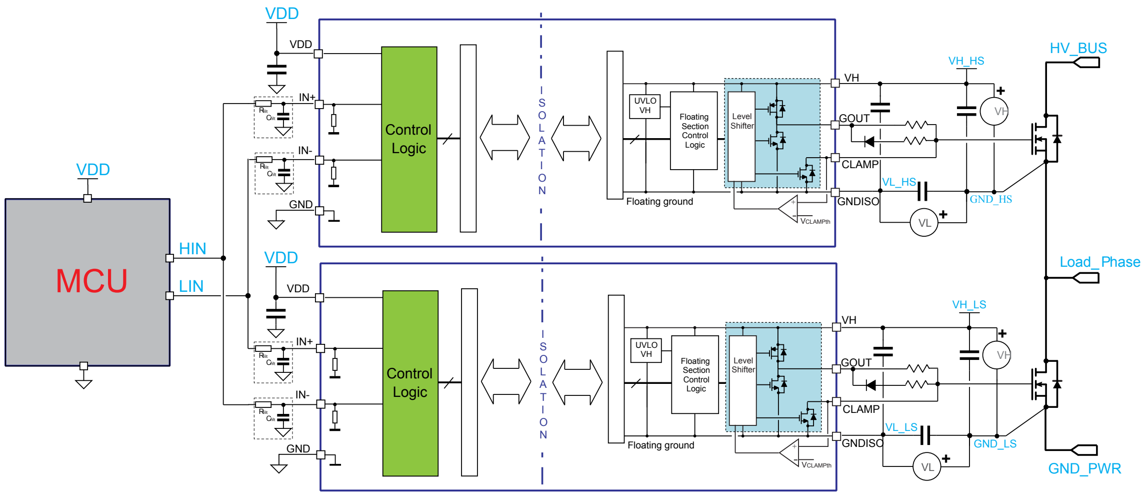


Figure 12. **Typical application diagram - Miller Clamp and negative gate driving**



8 Layout

8.1 Layout guidelines and considerations

In order to optimize the PCB layout, the following considerations should be taken into account:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pins. A 100 nF capacitor must be placed between VDD and GND and between VH and GNDISO, as close as possible to device pins, in order to filter high-frequency noise and spikes. In order to provide local storage for pulsed current, a second capacitor with a value between 1 μF and 10 μF should also be placed close to the supply pins.
- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver to minimize the gate loop area and inductance that might carry noise or cause ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

An example of STGAP2SICSC suggested PCB layout with main signals highlighted by different colors is shown in Figure 13 (see Figure 14 for reference schematic). It is recommended to follow this example for correct positioning and connection of filtering capacitors.

Figure 13. STGAP2SICSC suggested PCB layout: top and bottom

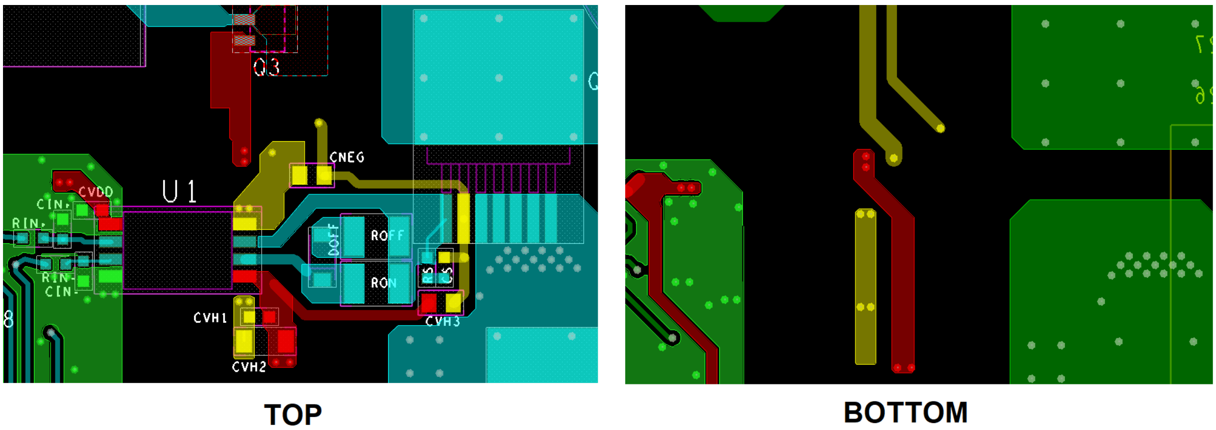
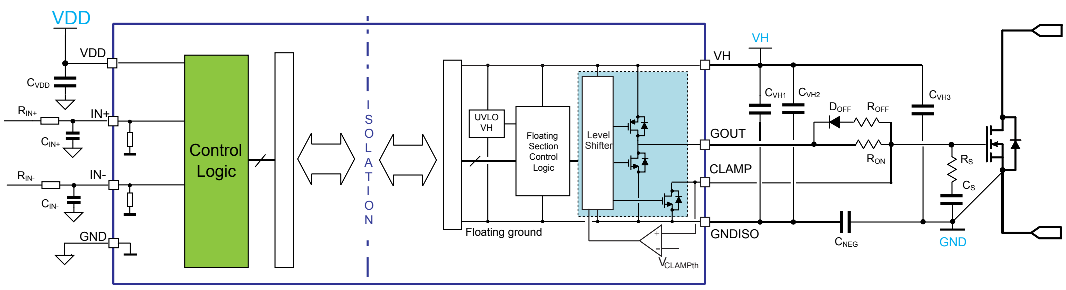


Figure 14. STGAP2SICSC reference schematic for suggested PCB layout



9 Testing and characterization information

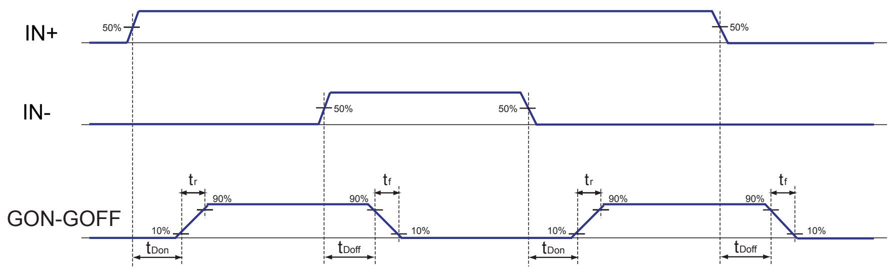


Figure 15. Timings definition

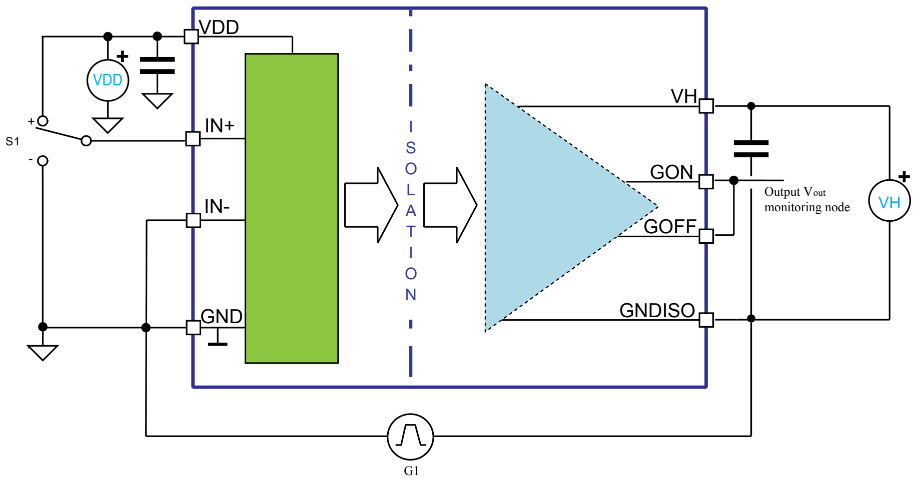


Figure 16. CMTI test circuit

10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

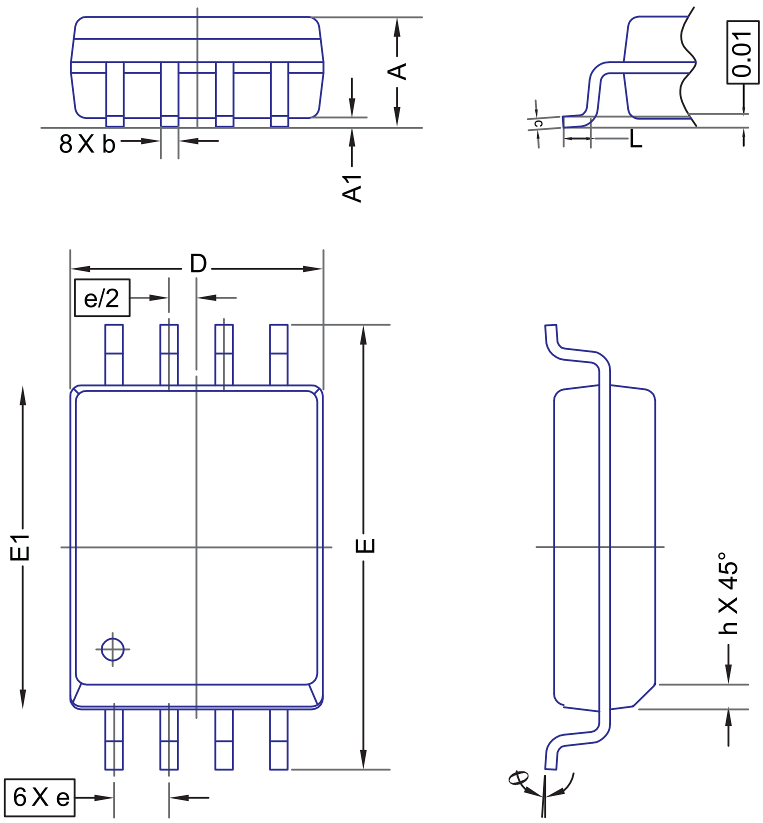
10.1 SO-8W package information

Table 9. SO-8W package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max
A	2.34		2.64
A1	0.1		0.3
b	0.3		0.51
c	0.2		0.33
D[(1)]	5.64		6.05
e	1.27 BSC		
E1	7.39		7.59
E	10.11		10.52
L	0.61		0.91
h	0.25		0.76
Θ	0°		8°
aaa	0.25		
bbb	0.25		
ccc	0.1		

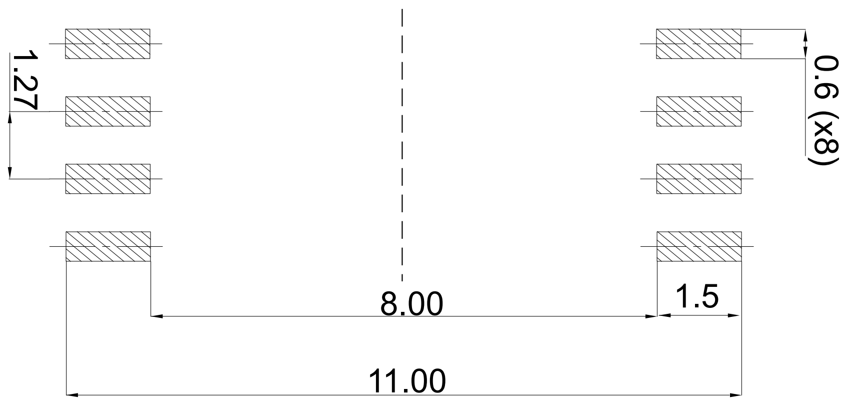
1. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.*

Figure 17. **SO-8W mechanical data**



10.2 SO-8W suggested land pattern

Figure 18. **SO-8W suggested land pattern**



11 Ordering information

Table 10. Device summary

Order code	Output configuration	Package marking	Package	Packing
STGAP2SICS	GON-GOFF	GAP2IS	SO-8W	Tube
STGAP2SICSTR	GON-GOFF	GAP2IS	SO-8W	Tape and Reel
STGAP2SICSCTR	GOUT-CLAMP	GAP2SIC	SO-8W	Tube
STGAP2SICSCTR	GOUT-CLAMP	GAP2SIC	SO-8W	Tape and Reel

Revision history

Table 11. Document revision history

Date	Version	Changes
10-Sep-2020	1	Initial release.
13-Aug-2021	2	Update VDD parameter in Table 3; update Isolation Resistance Test condition parameter in Section 5; update title of UL1577 section; change Figure 18 and Figure 12; updated Table 4; updated Driver buffer section and Standby in Table 5.
15-Oct-2021	3	Updated test condition in Table 5.
29-Sep-2022	4	Added UL file certification
27-Jan-2026	5	Added IEC 60747-17 certification: updated Section Features and Section 5; updated Cover image, Section 6.3, Section 8.2; added Section Applications. Updated Table 2 (T_{stg} symbol), Table 3 (added T_{amb}), and Table 10 (added tube order codes). Updated Figure 7, Figure 9, Figure 10, Figure 11, Figure 12.

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