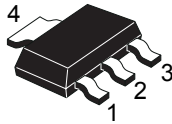
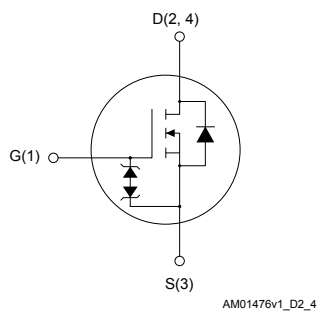


N-channel 400 V, 3.1 Ω typ., 1.8 A MDmesh K3 Power MOSFET in a SOT-223 package



SOT-223



Product status link

[STN3N40K3](#)

Product summary

Order code	STN3N40K3
Marking	3N40K3
Package	SOT-223
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STN3N40K3	400 V	3.4 Ω	1.8 A

- Extremely high dv/dt capability
- Improved diode reverse recovery characteristics
- Very low intrinsic capacitance
- Zener-protected
- 100% avalanche tested

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at $T_A = 25\text{ °C}$	1.8	A
	Drain current (continuous) at $T_A = 100\text{ °C}$	1	
$I_{DM}^{(1)}$	Drain current (pulsed)	7.2	A
P_{TOT}	Total power dissipation at $T_A = 25\text{ °C}$	3.3	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	1	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 1.8\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	38	°C/W

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	0.6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	45	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	400	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.9\text{ A}$	-	3.1	3.4	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	165	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{DS} = 0\text{ to }320\text{ V}$, $V_{GS} = 0\text{ V}$	-	9	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	14	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	10	-	Ω
Q_g	Total gate charge	$V_{DD} = 320\text{ V}$, $I_D = 1.8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 15. Test circuit for gate charge behavior)	-	9.5	-	nC
Q_{gs}	Gate-source charge		-	2	-	nC
Q_{gd}	Gate-drain charge		-	6	-	nC

- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.
- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}$, $I_D = 0.6\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	7	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	18	-	ns
t_f	Fall time		-	14	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	1.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	7.2	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 1.8\text{ A}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$	-	145	-	ns
Q_{rr}	Reverse recovery charge		-	490	-	nC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	7	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 1.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$	-	166	-	ns
Q_{rr}	Reverse recovery charge		-	580	-	nC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	7	-	A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

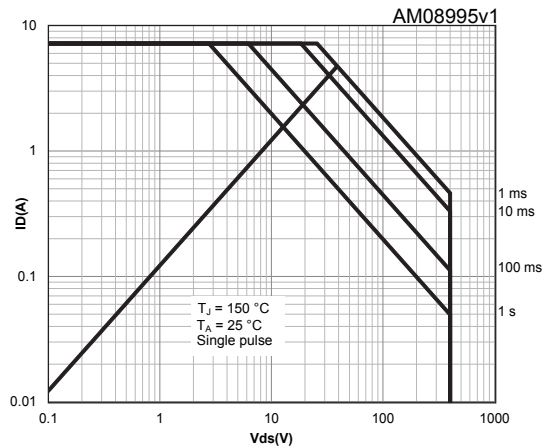


Figure 2. Normalized transient thermal impedance

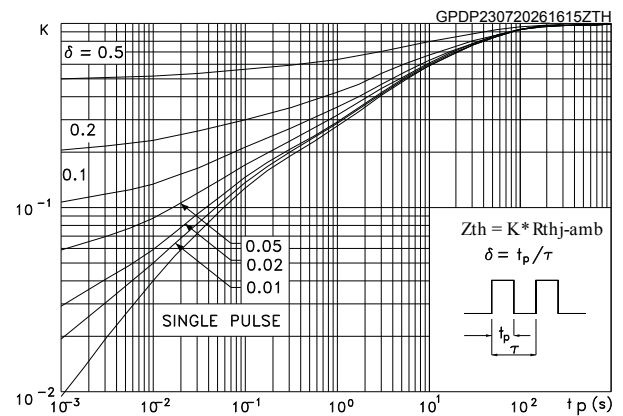


Figure 3. Typical output characteristics

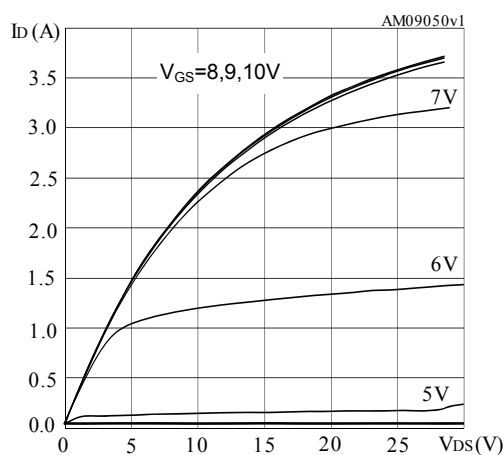


Figure 4. Typical transfer characteristics

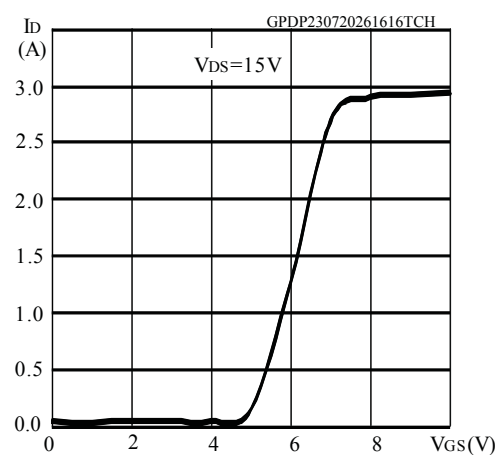


Figure 5. Typical gate charge characteristics

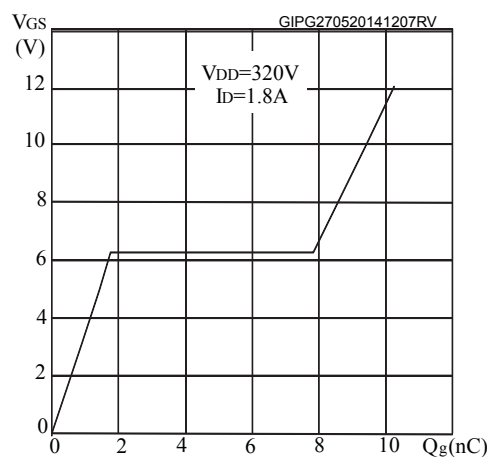


Figure 6. Typical drain-source on-resistance

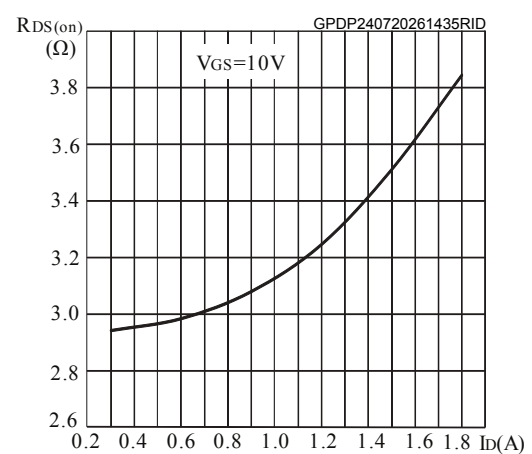


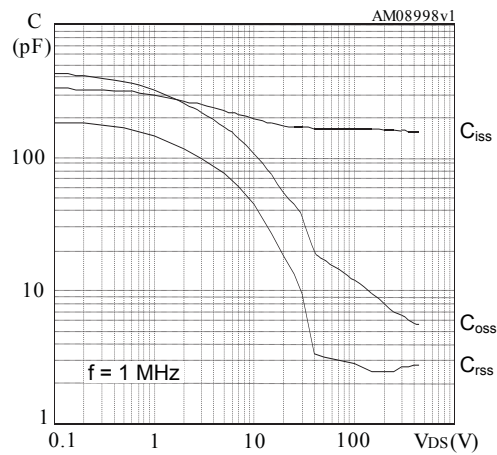
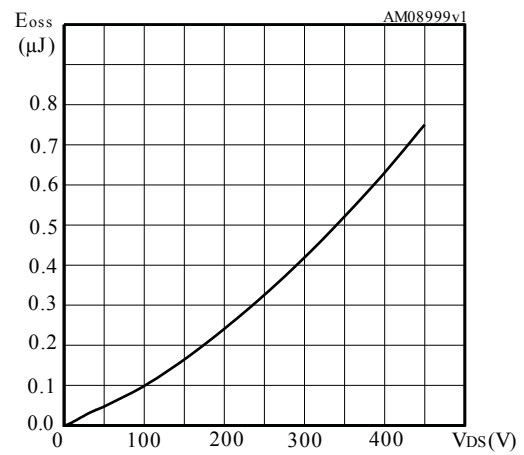
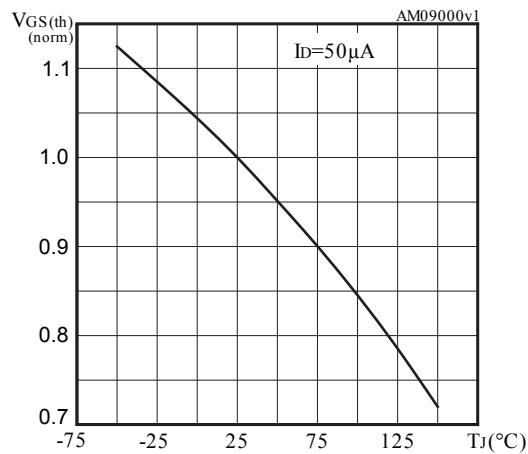
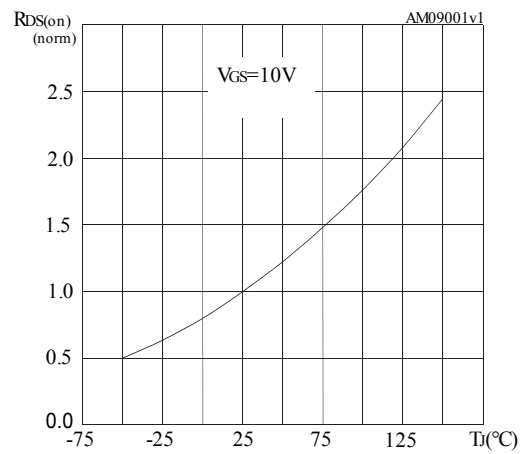
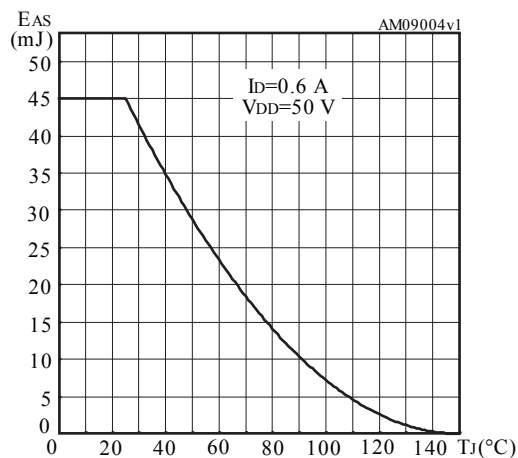
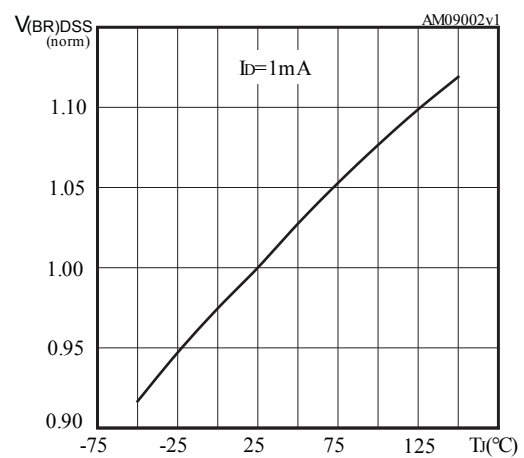
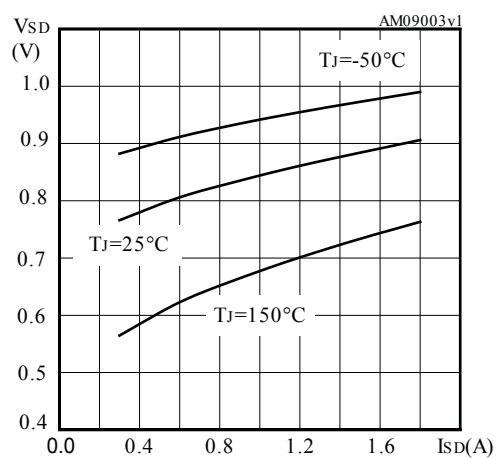
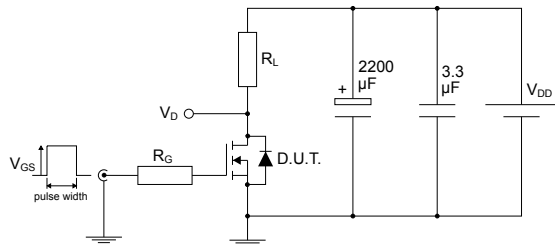
Figure 7. Typical capacitance characteristics

Figure 8. Typical output capacitance stored energy

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Maximum avalanche energy vs temperature

Figure 12. Normalized breakdown voltage vs temperature


Figure 13. Typical reverse diode forward characteristics



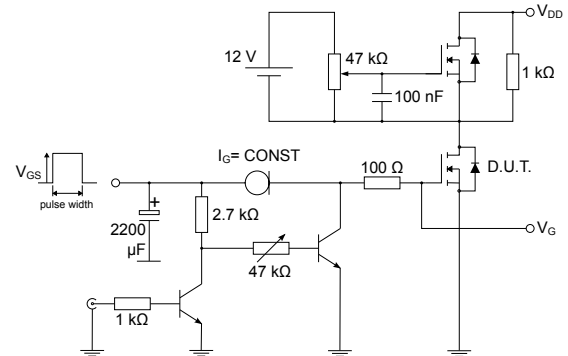
3 Test circuits

Figure 14. Test circuit for resistive load switching times



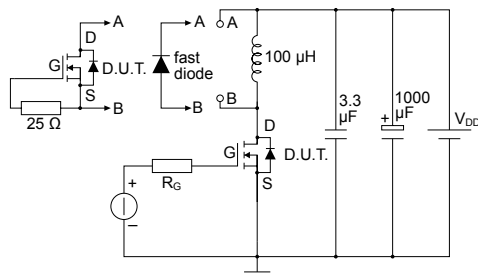
AM01468v1

Figure 15. Test circuit for gate charge behavior



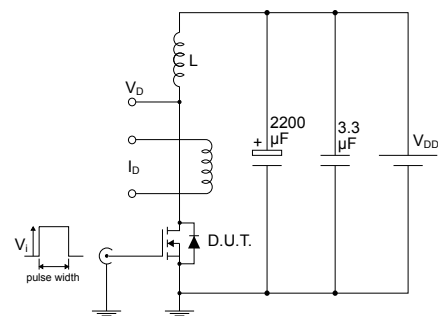
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Figure 16. Test circuit for inductive load switching and diode recovery times



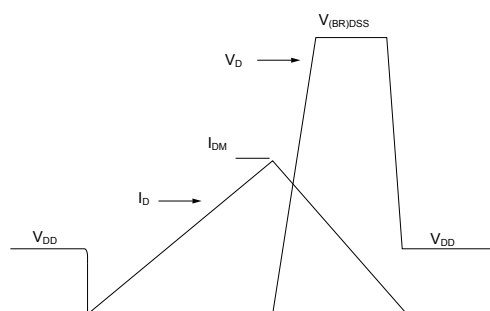
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Figure 17. Unclamped inductive load test circuit



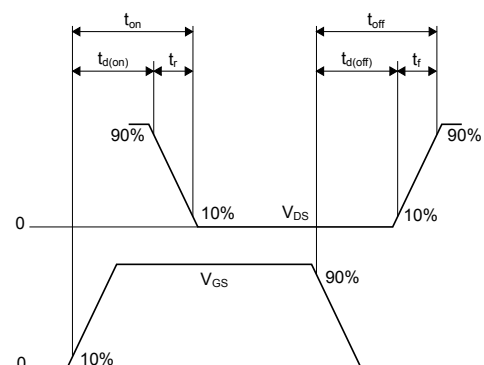
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



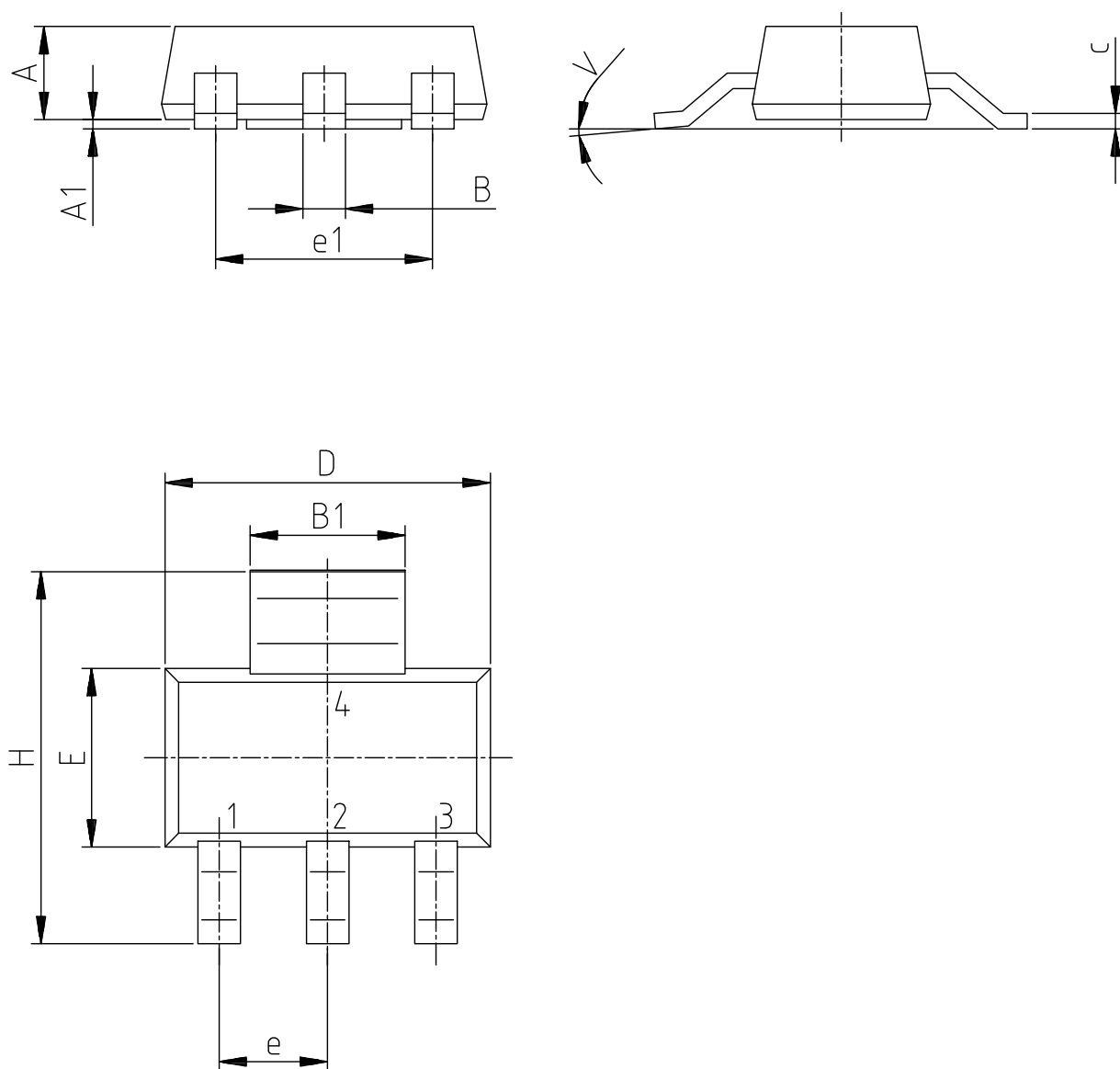
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT-223 package information

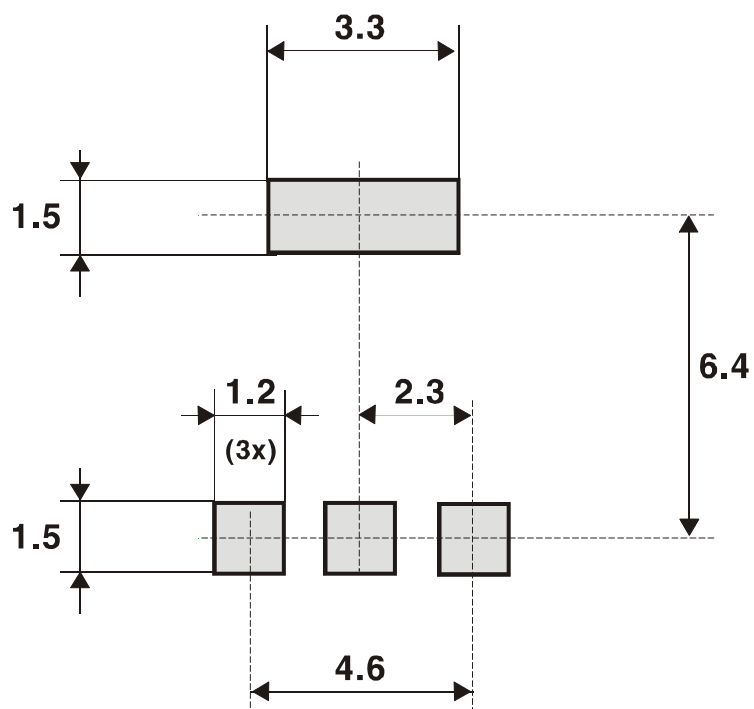
Figure 20. SOT-223 package outline



0046067_15

Table 8. SOT-223 package mechanical data

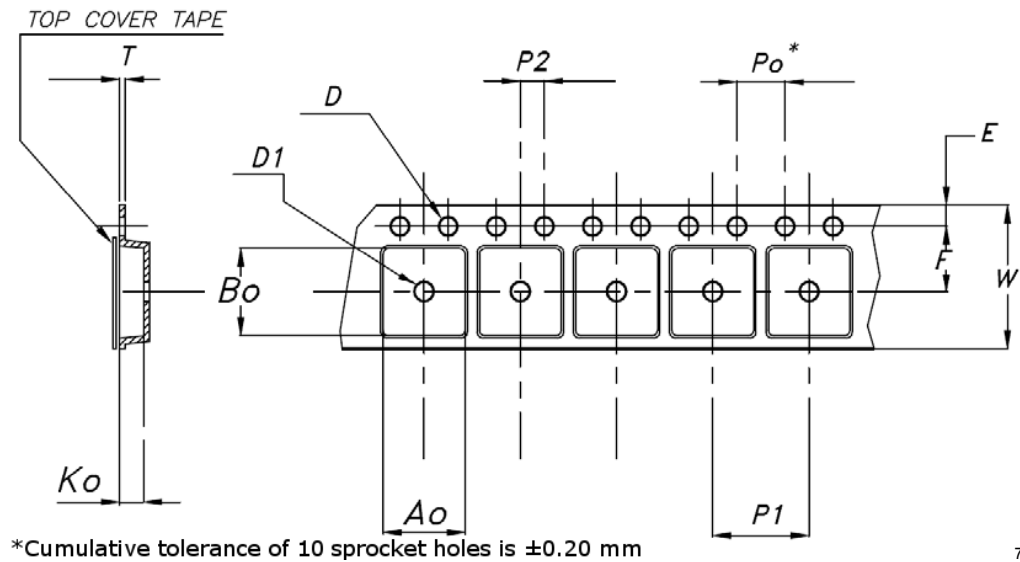
Dim.	mm		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V			10 deg
A1	0.02		0.1

Figure 21. SOT-223 recommended footprint (dimensions are in mm)


0046067_15

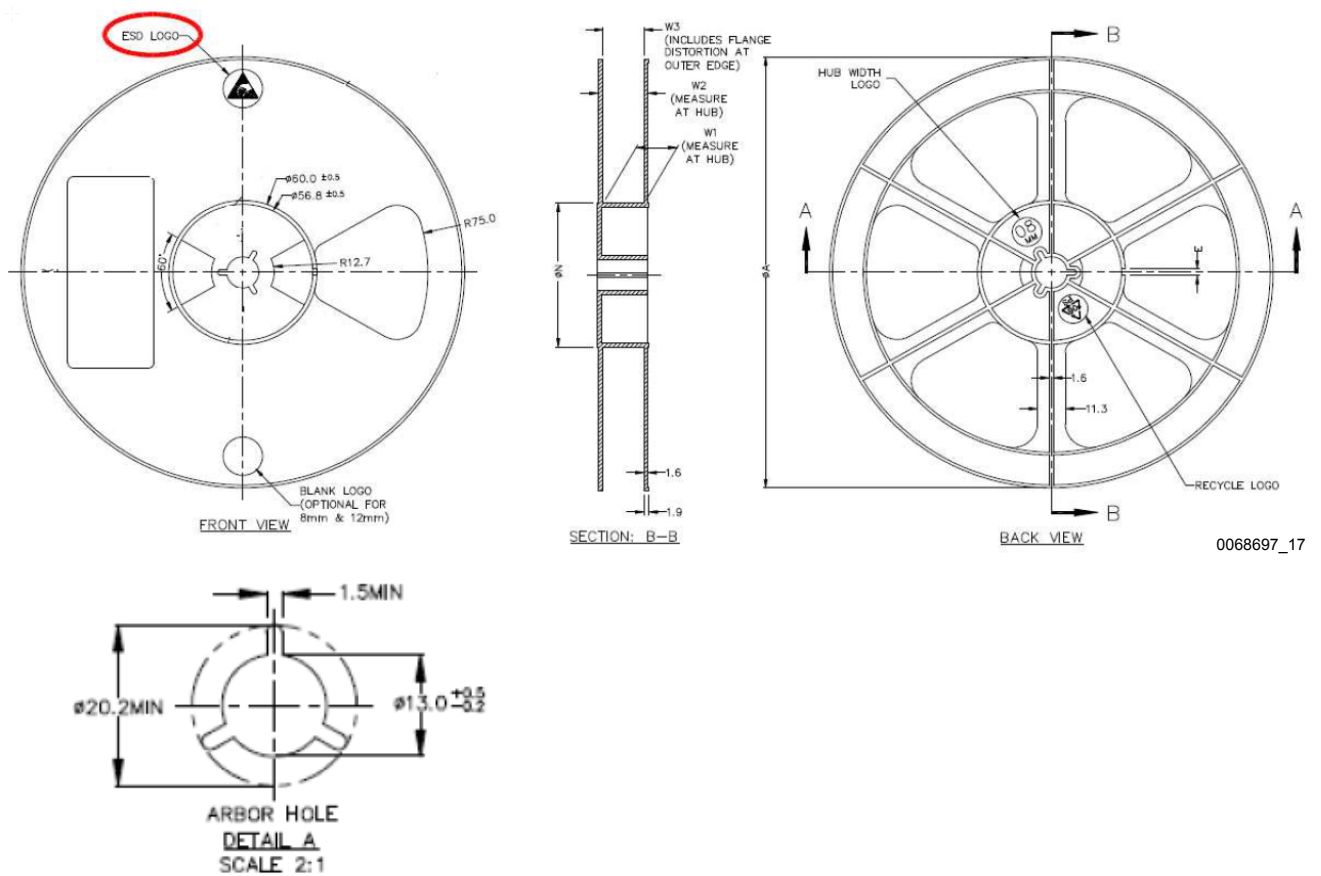
4.2 SOT-223 packing information

Figure 22. SOT-223 tape outline



7737436_3

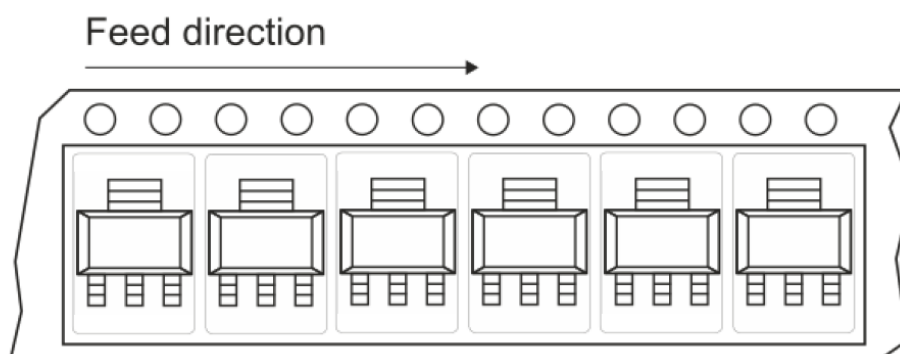
Figure 23. SOT-223 reel outline



0068697_17

Table 9. SOT-223 tape and reel mechanical data

Tape				Tape		
Dim.	mm			Dim.	mm	
	Min.	Typ.	Max.		Min.	Max.
A0	6.75	6.85	6.95	A		180
B0	7.30	7.40	7.50	N	60	
K0	1.80	1.90	2.00	W1		12.4
F	5.40	5.50	5.60	W2		18.4
E	1.65	1.75	1.85	W3	11.9	15.4
W	11.7	12.0	12.3			
P2	1.90	2.00	2.10	Base quantity pcs		1000
P0	3.90	4.00	4.10	Bulk quantity pcs		1000
P1	7.90	8.00	8.10			
T	0.25	0.30	0.35			
DΦ	1.50	1.55	1.60			
D1Φ	1.50	1.60	1.70			

Figure 24. SOT-223 package orientation in carrier tape


0050115_20

Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Jun-2010	1	First release.
08-Apr-2011	2	Document status promoted from preliminary data to datasheet.
06-Jun-2014	3	Updated silhouette, features and <i>Figure 1: Internal schematic diagram</i> in cover page. Updated <i>Table 2: Absolute maximum ratings</i> , <i>Table 3: Thermal data</i> , and <i>Table 4: On /off states</i> . Updated <i>Figure 2: Safe operating area</i> and <i>Figure 6: Gate charge vs gate-source voltage</i> . Updated <i>Section 4: Package mechanical data</i> . Minor text changes.
24-Jul-2026	4	Updated <i>Section 4: Package information</i> . Minor text changes.

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