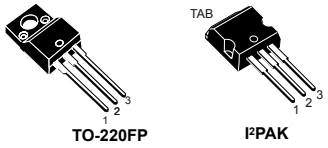
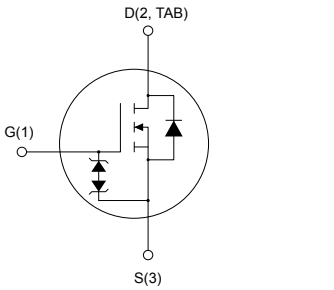
STF4N62K3, STI4N62K3, STU4N62K3

Datasheet

N-channel 620 V, 1.7 Ω typ., 3.8 A MDmesh K3 Power MOSFET in a TO-220FP, I²PAK and IPAK packages





Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STF4N62K3	620 V	2 Ω	3.8 A
STI4N62K3			
STU4N62K3			

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These MDmesh K3 Power MOSFETs are the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Product status link
STF4N62K3
STI4N62K3
STU4N62K3

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	IPAK I²PAK	
V_{DS}	Drain-source voltage	620		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	3.8		A
	Drain current (continuous) at T_C = 100 °C	2		
I_{DM}(1)	Drain current (pulsed)	15.2		A
P_{TOT}	Total power dissipation at T_C = 25 °C	25	70	W
dv/dt(2)	Peak diode recovery voltage slope	12		V/ns
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.5		kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	-	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Maximum operating junction temperature	150		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 3.8 A, di/dt = 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 496 V.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	I²PAK	IPAK	
R_{thJC}	Thermal resistance, junction-to-case	5	1.79		°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		100	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	3.8	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	115	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	620	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 620 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 620 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.9 A	-	1.7	2	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	550	-	pF
C_{oss}	Output capacitance		-	42	-	pF
C_{rss}	Reverse transfer capacitance		-	7	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 496 V, V_{GS} = 0 V	-	27	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	2(2)	5	10(2)	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 3.8 A, V_{GS} = 0 to 10 V (see the Figure 19. Test circuit for gate charge behavior)	-	22	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	13	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Specified by design, not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1.9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 18. Test circuit for resistive load switching times and Figure 23. Switching time waveform)	-	10	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	29	-	ns
t_f	Fall time		-	19	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	3.8	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	15.2	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 3.8 A	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 3.8 A, di/dt = 100 A/µs, V_{DD} = 60 V (see the Figure 20. Test circuit for inductive load switching and diode recovery times)	-	220	-	ns
Q_{rr}	Reverse recovery charge		-	1.4	-	µC
I_{RRM}	Reverse recovery current		-	13	-	A
t_{rr}	Reverse recovery time	I_{SD} = 3.8 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see the Figure 20. Test circuit for inductive load switching and diode recovery times)	-	270	-	ns
Q_{rr}	Reverse recovery charge		-	1.9	-	µC
I_{RRM}	Reverse recovery current		-	14	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP

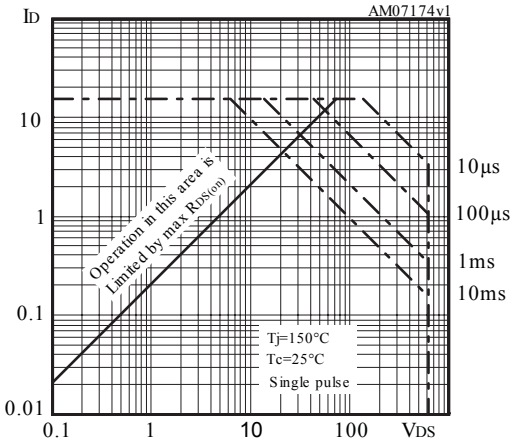


Figure 2. Normalized transient thermal impedance for TO-220FP

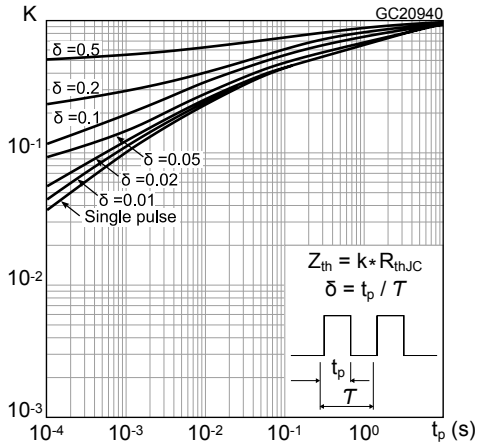


Figure 3. Safe operating area for I²PAK

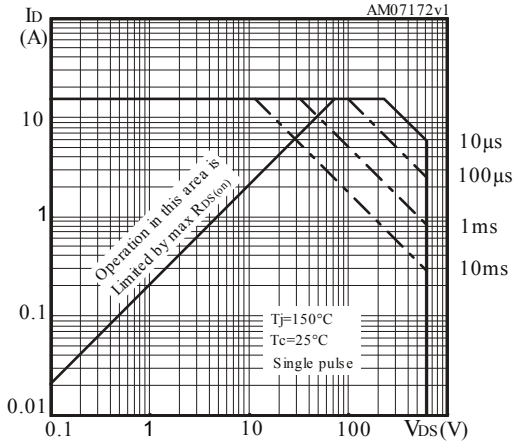


Figure 4. Normalized transient thermal impedance for I²PAK

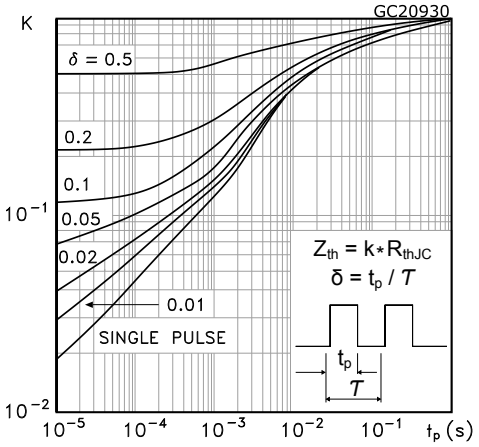


Figure 5. Safe operating area for IPAK

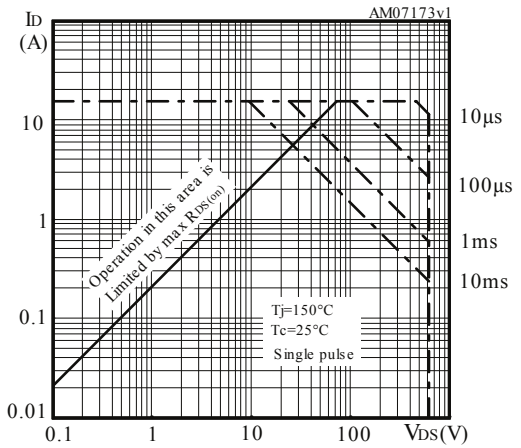


Figure 6. Normalized transient thermal impedance for IPAK

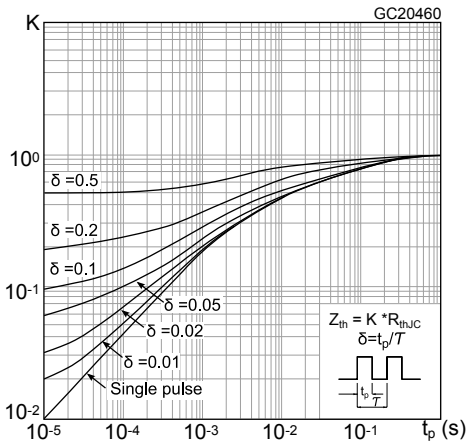


Figure 7. Typical output characteristics

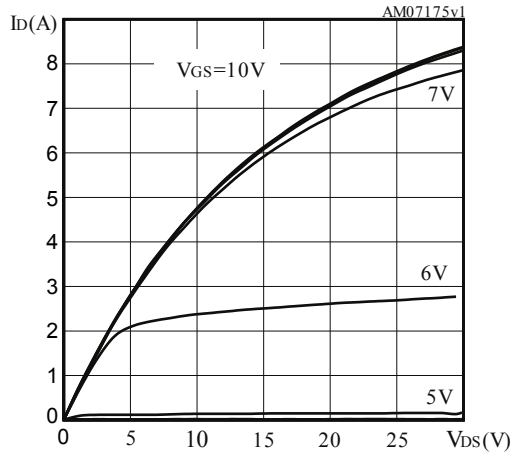


Figure 8. Typical transfer characteristics

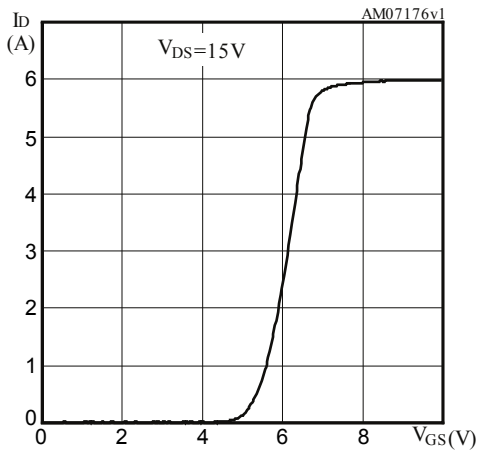


Figure 9. Typical gate charge characteristics

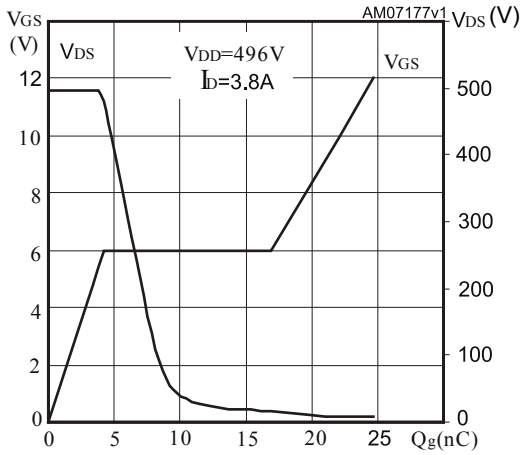


Figure 10. Typical drain-source on-resistance

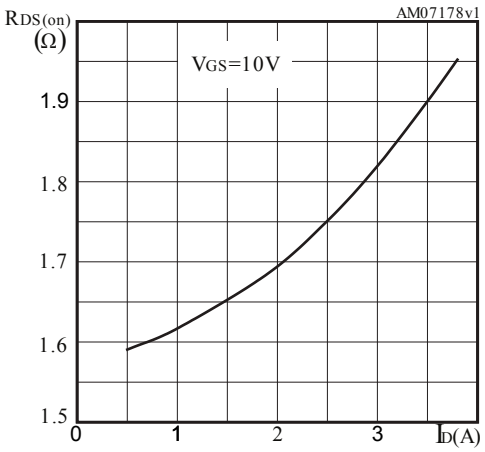


Figure 11. Typical capacitance characteristics

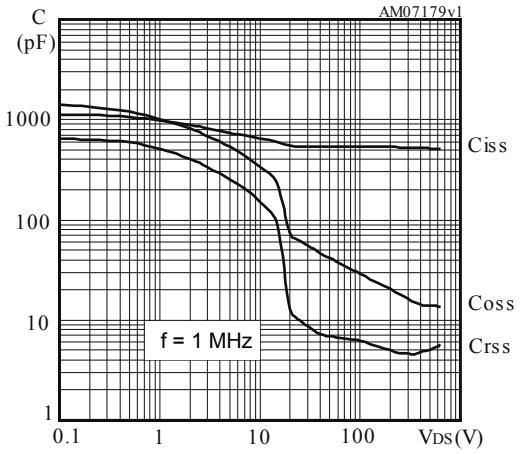


Figure 12. Typical output capacitance stored energy

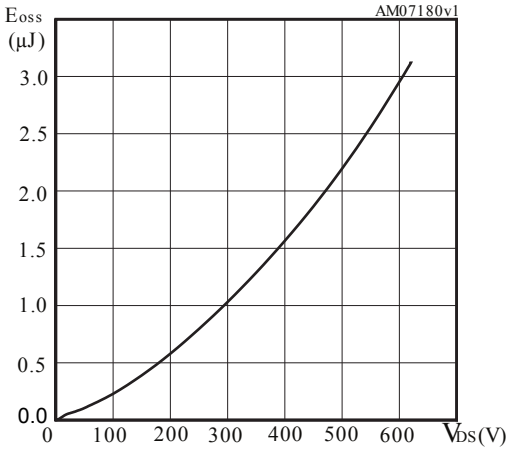


Figure 13. Normalized gate threshold vs temperature

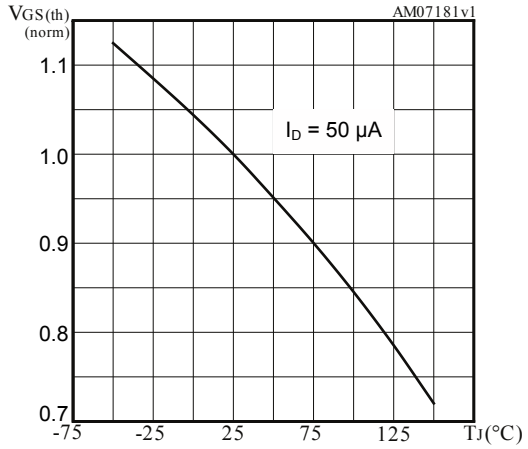


Figure 14. Normalized on-resistance vs temperature

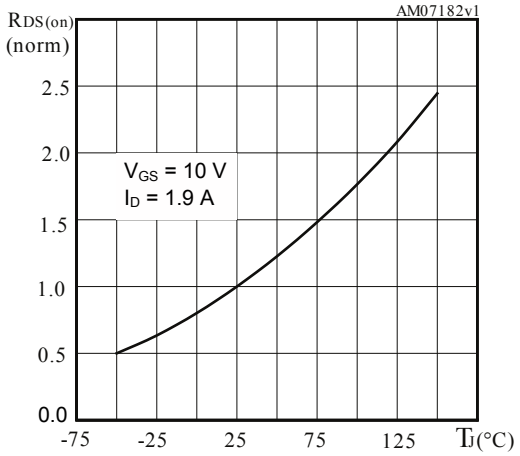


Figure 15. Maximum avalanche energy vs temperature

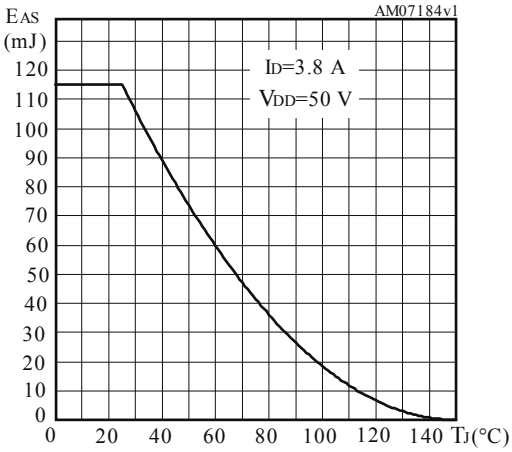


Figure 16. Normalized breakdown voltage vs temperature

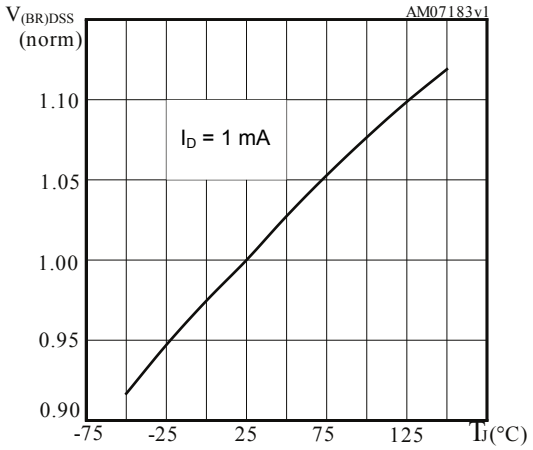
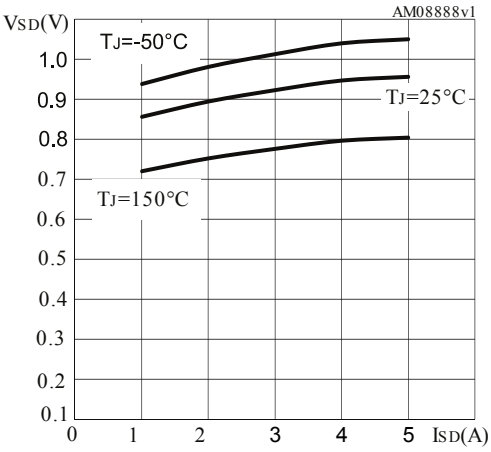


Figure 17. Typical reverse diode forward characteristics



3 Test circuits

Figure 18. Test circuit for resistive load switching times

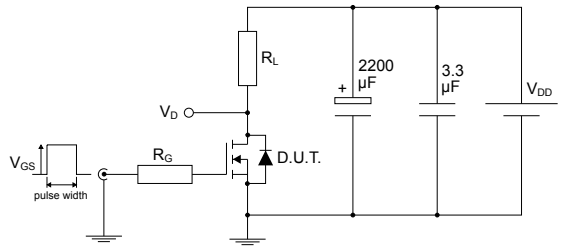


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Figure 19. Test circuit for gate charge behavior

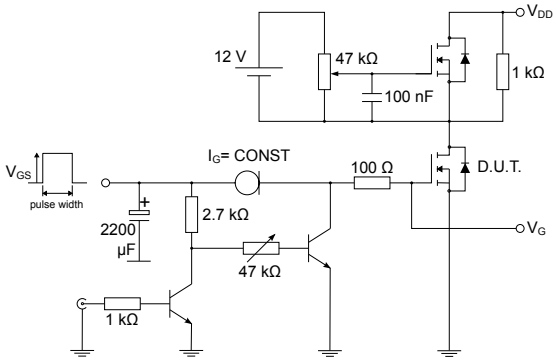

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Figure 20. Test circuit for inductive load switching and diode recovery times

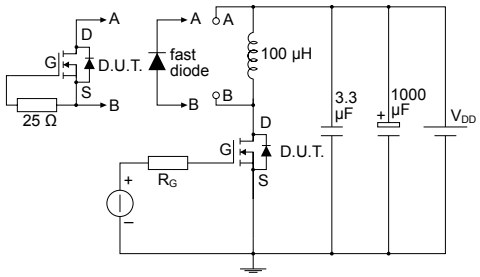

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Figure 21. Unclamped inductive load test circuit

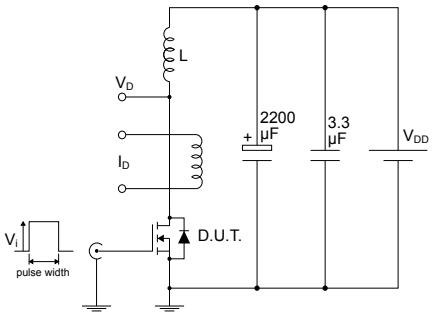

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Figure 22. Unclamped inductive waveform

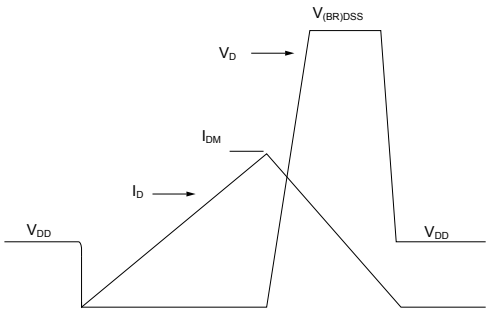

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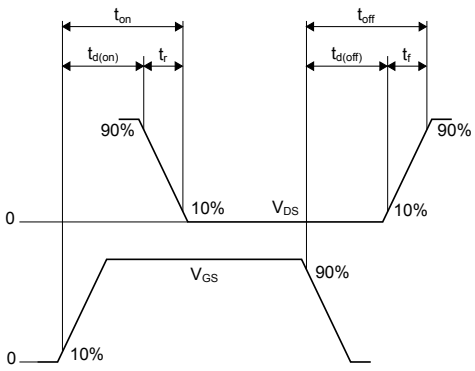
Figure 23. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 24. TO-220FP type B package outline

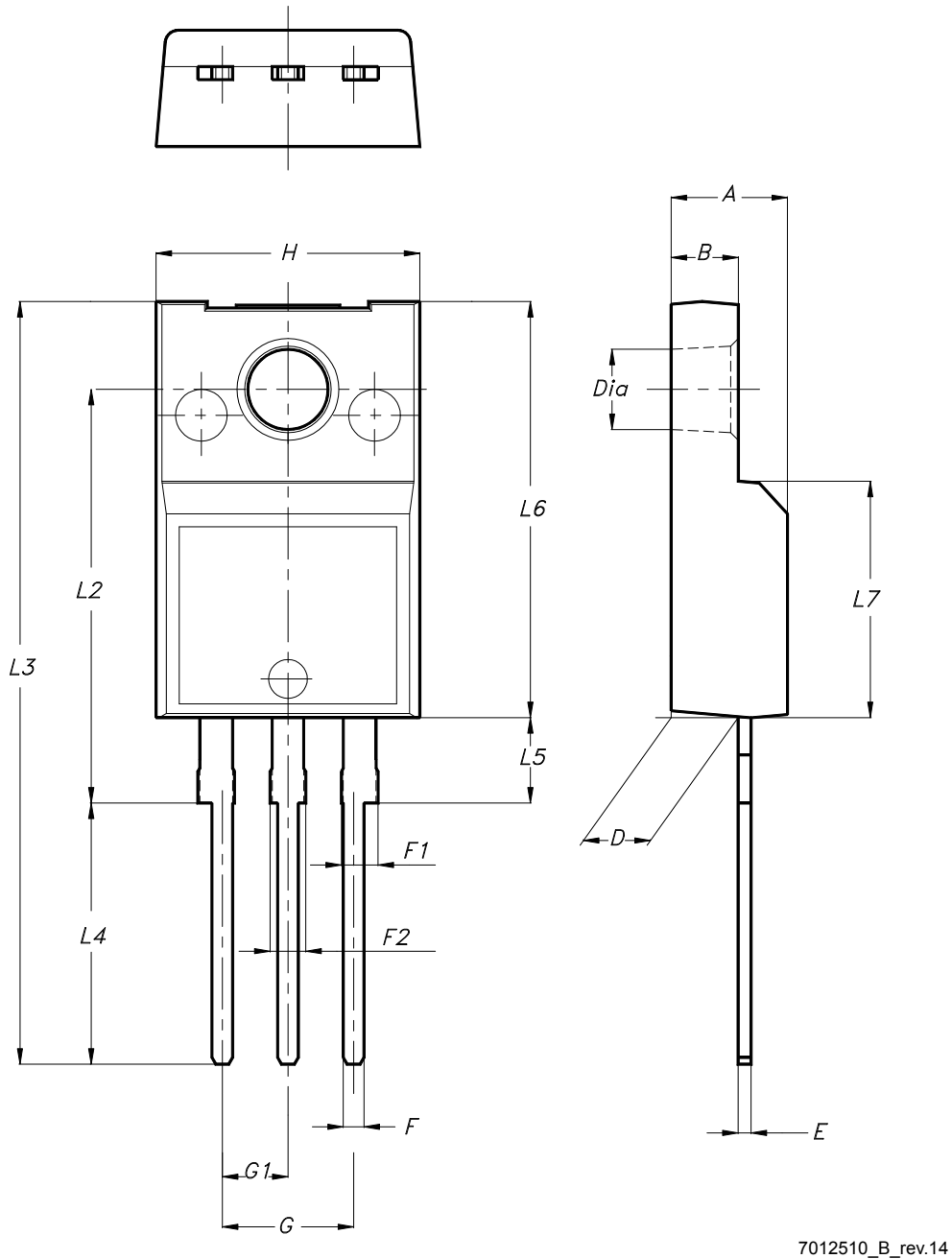

Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 I²PAK package information

Figure 25. I²PAK package outline

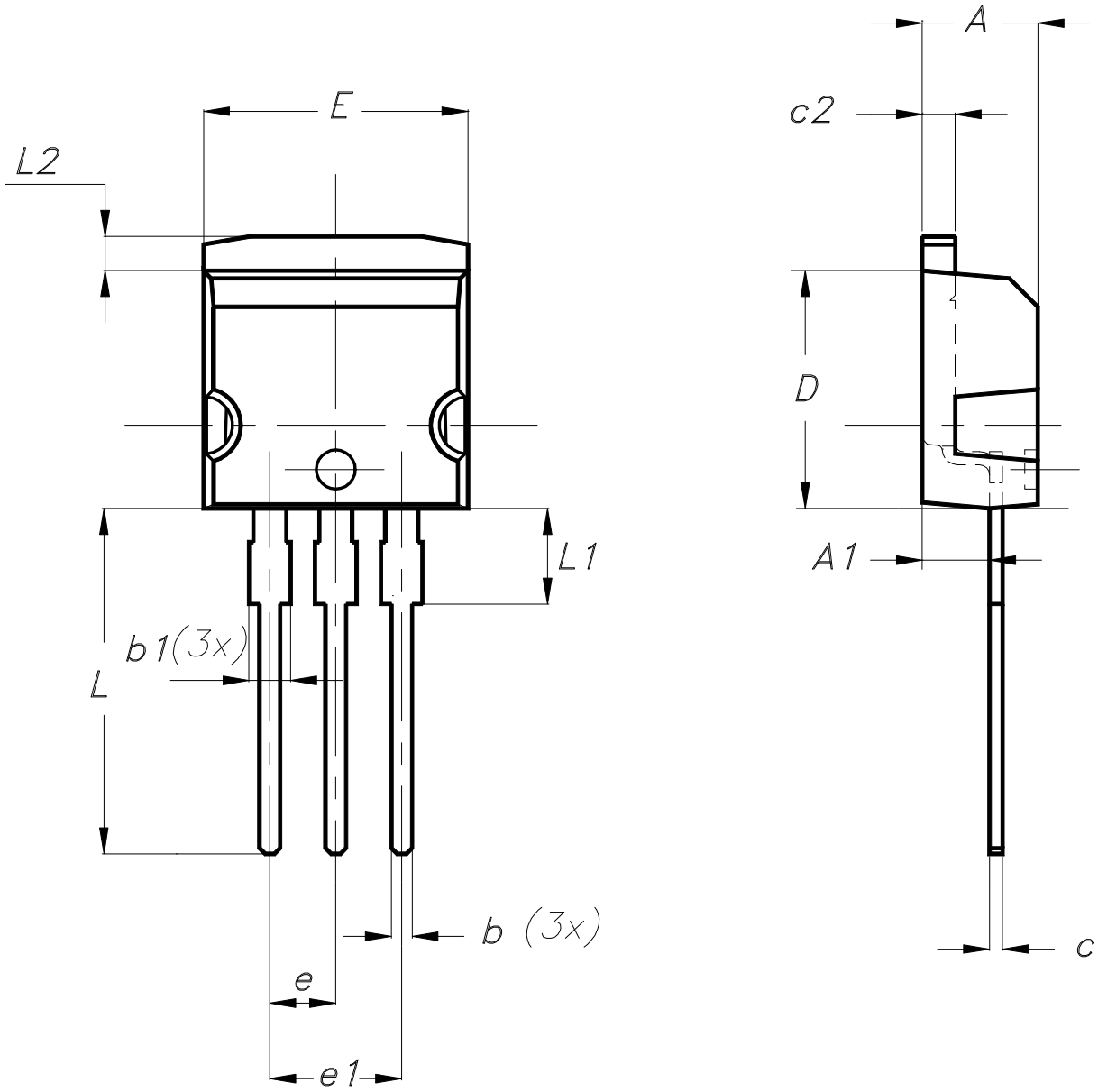

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Table 9. I²PAK package mechanical data

Dim.	mm	
	Min.	Max.
A	4.40	4.60
A1	2.40	2.72
b	0.61	0.88
b1	1.14	1.70
c	0.49	0.70
c2	1.23	1.32
D	8.95	9.35
e	2.40	2.70
e1	4.95	5.15
E	10.00	10.40
L	13.00	14.00
L1	3.50	3.93
L2	1.27	1.40

4.3 IPAK (TO-251) type A package information

Figure 26. **IPAK (TO-251) type A package outline**

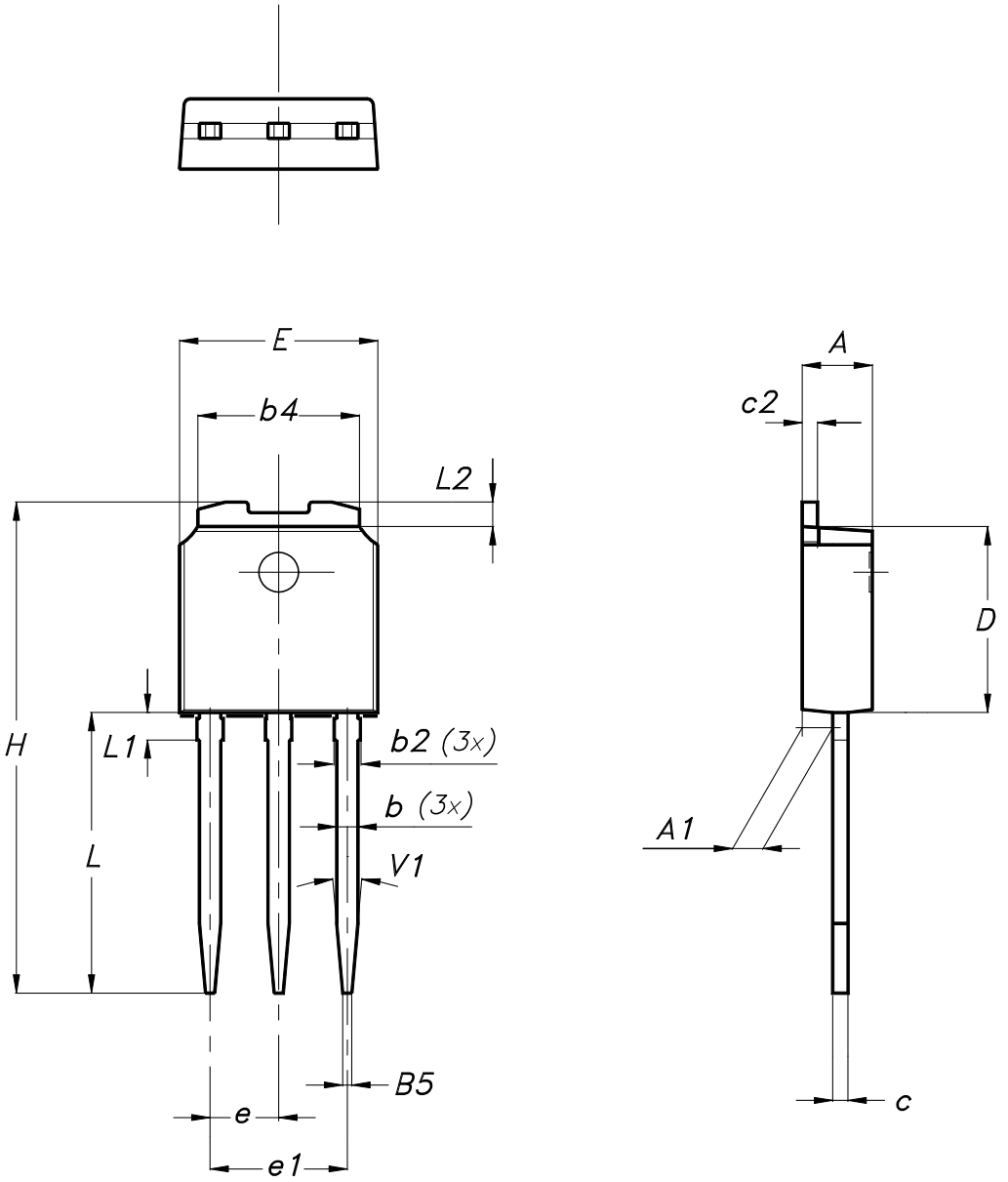

Table 10. **IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Ordering information

Table 11. **Order codes**

Order codes	Marking	Package	Packing
STF4N62K3	4N62K3	TO-220FP	Tube
STI4N62K3		I²PAK	
STU4N62K3		IPAK	

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
05-May-2010	1	First release.
16-Dec-2010	2	Document status promoted from preliminary data to datasheet.
27-Mar-2012	3	Inserted max and min. values for R_G in *Table 5*. Updated *Section 4: Package mechanical data*.
07-Aug-2012	4	Added package, mechanical data: I²PAKFP. Updated *Table 1: Device summary*, *Table 2: Absolute maximum ratings*, *Table 3: Thermal data*, *Table 4: On /off states*, *Table 13: IPAK (TO-251) mechanical data* and *Figure 29: IPAK (TO-251) drawing*. Minor text changes.
27-Jan-2026	5	Removed order code STFI4N62K3 and STP4N62K3. Updated Section 4: Package information. Minor text changes.

Contents