



STM32WB07xC and STM32WB06xC devices errata

Applicability

This document applies to the part numbers of STM32WB07xC and STM32WB06xC devices and the device variants as stated in this page.

It gives a summary and a description of the device errata, with respect to the device datasheet and reference manual RM0530. Deviation of the real device behavior from the intended device behavior is considered to be a device limitation. Deviation of the description in the reference manual or the datasheet from the intended device behavior is considered to be a documentation erratum. The term “*errata*” applies both to limitations and documentation errata.

Table 1. Device summary

Reference	Part numbers
STM32WB06xC	STM32WB06KC, STM32WB06CC
STM32WB07xC	STM32WB07KC, STM32WB07CC

Table 2. Device variants

Reference	Silicon revision codes	
	Device marking ⁽²⁾	DIE_ID ⁽¹⁾
STM32WB06xC, STM32WB07xC	9	0x120

1. Register system controller (SYSCFG) - DIE_ID register.

2. Refer to the device datasheet for how to identify this code on different types of packages.

1 Summary of device errata

The following table gives a quick reference to the STM32WB07xC and STM32WB06xC device limitations and their status:

A	Limitation applicable. Workaround available
N	Limitation applicable. No workaround available
P	Limitation applicable. Partial workaround available
-	Limitation not applicable.

Applicability of a workaround may depend on specific conditions of target application. Adoption of a workaround may cause restrictions to target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the function concerned.

Table 3. Summary of device limitations

Function	Section	Limitation	Status
			Rev. 9
System	2.2.1	Host wake-up source does not wake the device from Deepstop	A
	2.2.2	HSE phase noise	P
	2.2.3	SMPS with BOM1 does not work properly at 4 MHz	A
Radio system	2.3.1	Unsupported system and Bluetooth LE clock configuration combinations	N
ADC	2.5.1	ADC occasional mode does not work	P
GPIO	2.4.1	Activity on some GPIOs may affect the RF performance	P
RTC	2.6.1	RTC key lost	A
	2.6.2	RTC alarm is not able internally to wake up the device from Deepstop mode	A
	2.6.3	RTC interrupt not triggered in Run mode	P

The following table gives a quick reference to the documentation errata.

Table 4. Summary of device documentation errata

Function	Section	Documentation erratum
GPIO	2.4.2	I/Os are wrongly stated as 5 V tolerant

2 Description of device errata

The following sections describe the errata of the applicable devices and provide a workaround where available. They are grouped by device functions.

The applicable devices are based on Arm® Cortex® core.

arm

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2.1 Core

Reference manual and errata notice for the Arm® Cortex®-M0+ core revision r0p1 is available from <http://infocenter.arm.com>.

2.2 System

2.2.1 Host wake-up source does not wake the device from Deepstop

Description

The wake-up block of the radio manages a Host wake-up timer in parallel to the Bluetooth® wake-up timer. This timer can be used as an additional slow clock timer available in the SoC to exit the device from a Deepstop without launching any Bluetooth sequence.

This timer does not raise any wake-up request to the power controller of the device.

Workaround

Use the RTC block to wake up the system. A software workaround is provided in the STM32WB0 SW package.

2.2.2 HSE phase noise

Description

HSE phase noise is observed when the high speed external IO current control register is set to value > 4 (max. 0.61 mA/V).

Workaround

High speed external IO current control register setting to a value < 5 is highly recommended (RCC_RFSWHSECR register, bits GMC[2:0]).

2.2.3 SMPS with BOM1 does not work properly at 4 MHz

Description

When using the bill of material BOM1 (inductor of 1.5 µH and capacitor of 2.2 µF), and when the frequency switching (Fs) is set at 4 MHz, the SMPS cannot deliver the right output voltage.

Workaround

Set the frequency switching to 8 MHz if the BOM1 is required for low-profile-height components.

If no low-profile-height components are required, use the standard bill of material BOM3 (inductor of 10 µH and capacitor of 4.7 µF).

2.3 Radio system

2.3.1 Unsupported system and Bluetooth LE clock configuration combinations

Description

The following system and Bluetooth Low Energy (LE) clock configuration combinations are not supported

1. System_Clock = 32 MHz and Ble_Clock = 32 MHz
2. System_Clock = 16 MHz and Ble_Clock = 16 MHz

Workaround

None.

2.4 GPIO

2.4.1 Activity on some GPIOs may affect the RF performance

Description

RF performance can be degraded in the presence of one of the following conditions:

- VFQFPN32 package only: toggling activity on PB14 and PB15 during RF communication
- VFQFPN32 and WLCSP49 packages: GPIO tracks are routed close to OSCIN/OSCOUT pins and toggling activity on those GPIOs during RF communications.

The user might experience a high packet error rate during RF communications.

Workaround

- VFQFPN32 package only: avoid toggling PB14 and PB15 (input or output) during RF communications.
- VFQFPN32 and WLCSP49 packages: avoid routing GPIO tracks close to OSCIN/OSCOUT tracks, if they are toggling during RF communications.

2.4.2 I/Os are wrongly stated as 5 V tolerant

Description

Some datasheet revisions may wrongly state that the I/Os are 5 V tolerant, by indicating “FT” in the “I/O structure” column of the “Pin description” table.

Some reference manual revisions show the figures “Basic structure of a mixed analog/digital five-volt tolerant I/O port bit” and “Basic structure of a digital only five-volt tolerant I/O port bit”. However, these figures are not applicable.

These errors have been corrected in DS14676 revision 6, in RM0530 revision 4, and all the later documents revisions.

Workaround

No application workaround is applicable.

2.5 ADC

2.5.1 ADC occasional mode does not work

Description

The occasional mode of the ADC allows catching one sample of the Vbat or the temperature sensor during an analog audio mode or full mode sequence. Since the setup time of the temperature sensor is too high and sampling only the first value provides a wrong value, the measure is good only from the second sample.

The temperature sensor occasional mode strategy (doing one measure among a continuous flow of measurements on another channel) does not work

Workaround

Two possible options to insert a temperature measurement among other channel measurements are the following:

1. Sequence mode with a downsampling ratio =1
 - The sequence mode can be composed of up to 16 conversions
 - Use the ADC mode in continuous regular sequence mode, with a downsampling ratio =1
 - Program 14 times the channel that has to be continuously converted
 - Program 2 consecutive times, the thermal sensor
 - Read all data on the « DS_DATAOUT_REG » register
 - Discard the first measure of the thermal sensor
2. Sequence mode with a downsampling ratio different from 1
 - The sequence mode can be composed of up to 16 conversions
 - Use the ADC mode in continuous regular sequence mode, with a downsampling ratio from 4 to 128 (downsampling ratio =2 is not recommended)
 - Program 15 times the channel that has to be continuously converted
 - Program 1 time, the thermal sensor
 - Read all data on « DS_DATAOUT_REG »"

2.6 RTC

2.6.1 RTC key lost

Description

RTC loses the keys inserted to unlock the calendar register access when the device goes to deepstop mode, due to PRESETn that should come from rcc_v12o instead of rcc_v12i.

RTC calendar update functionality is affected when system wakes up from Deepstop mode.

Workaround

Rewrite the key in the write protect register (WPR) after a Deepstop.

2.6.2 RTC alarm is not able internally to wake up the device from Deepstop mode

Description

The RTC is able to run in Deepstop mode but it cannot generate an internal RTC alarm wake-up event. An RTC alarm cannot be used as an internal wake-up source when the device is in Deepstop mode.

Workaround

In software, output an RTC alarm on PA8 and use this as the wake-up pin from Deepstop mode.

2.6.3 RTC interrupt not triggered in Run mode

Description

The RTC interrupts might get lost in Run mode when the selected RTC clock source is LSI or LSE. The problem does not occur when the RTC clock source is CLK_16MHz/512.

RTC interrupts cannot be reliably used for real-time control functions, since some occurrences of RTC interrupts may be missed.

Note: Wakeup from Deepstop mode is not affected and RTC interrupt is always reliable in Deepstop mode.

Workaround

While in Run mode, do not use RTC interrupts, but instead use polling on the RTC_ISR register. Another possible option is to output the RTC alarm or wake-up on PA8 or PA9, and use one of these pins as an I/O interrupt pin.

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Revision history

Table 5. Document revision history

Date	Version	Changes
13-Jun-2024	1	Initial release.
31-Oct-2024	2	Added SMPS with BOM1 does not work properly at 4 MHz.
12-Aug-2026	3	Added I/Os are wrongly stated as 5 V tolerant.

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